

ZQA SOLE UMA SYSTEM DIAGRAM

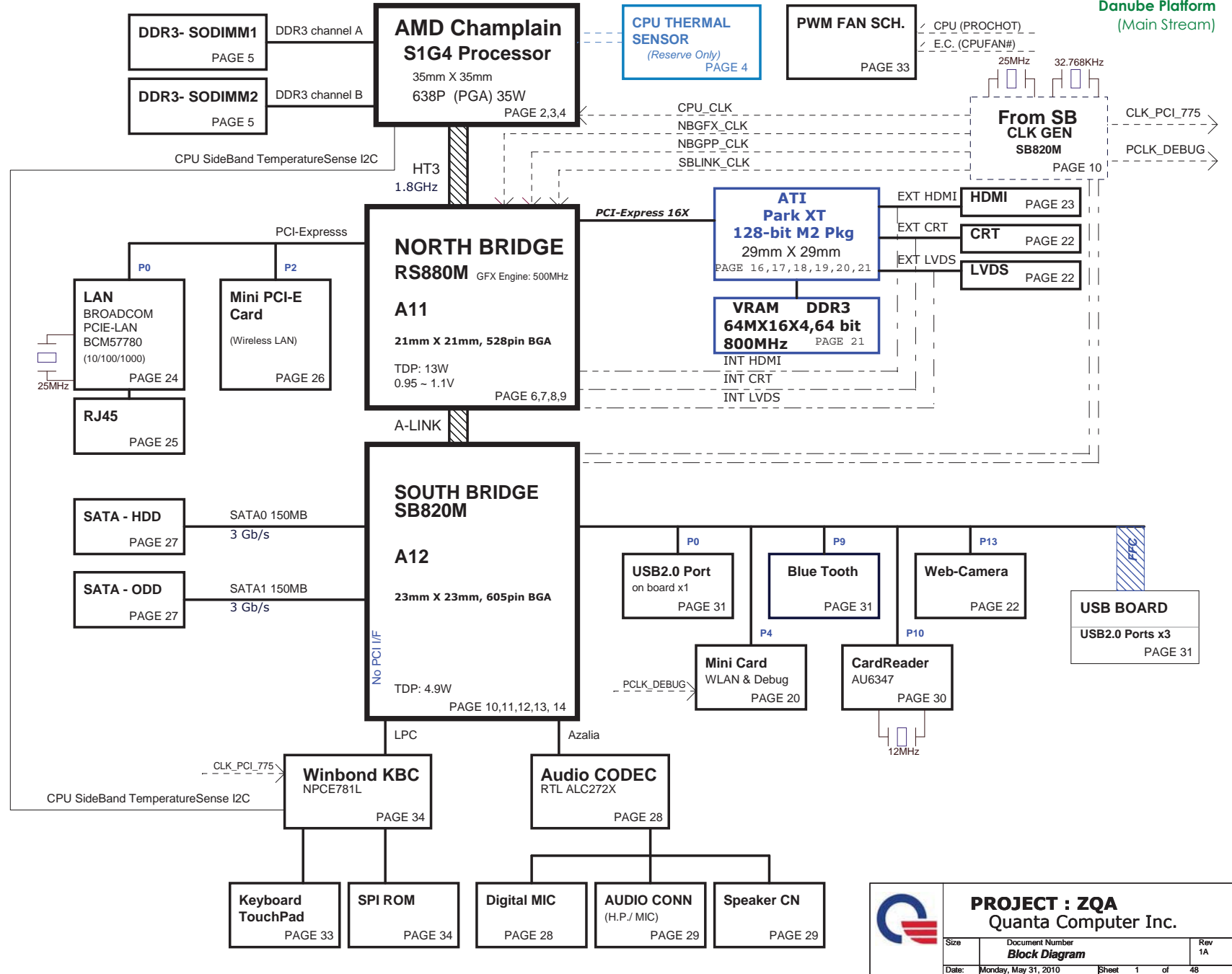


Danube Platform
(Main Stream)

PCB STACK UP

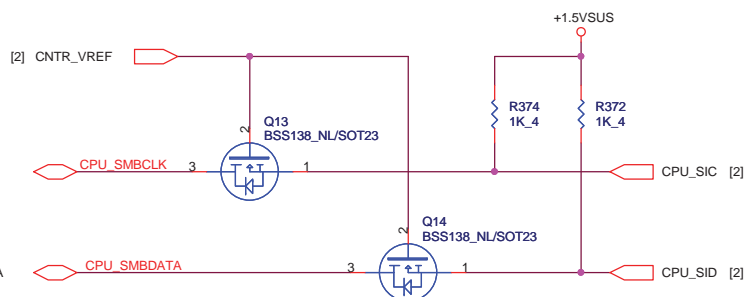
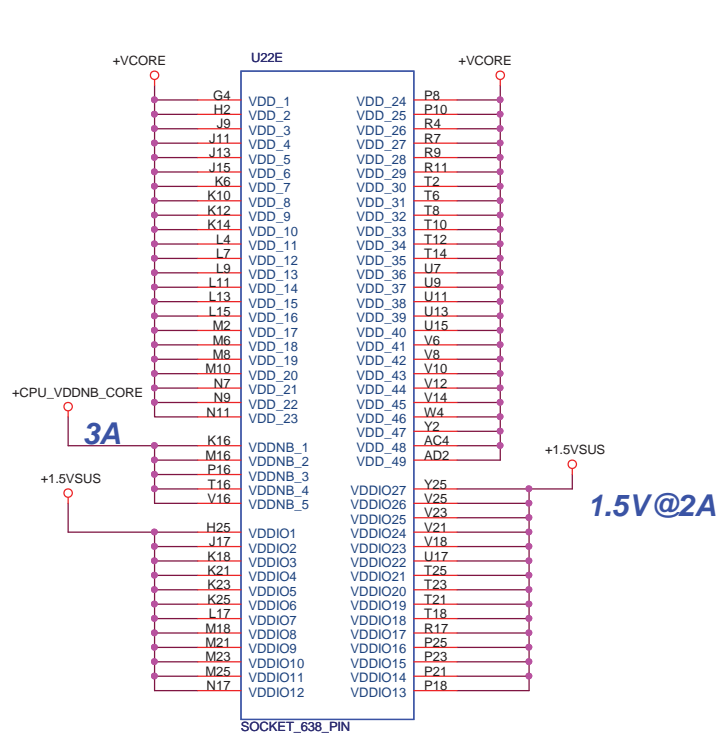
LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

IV@ -----> iGPU EV@ -----> dGPU
SPE@ -----> Option Notice

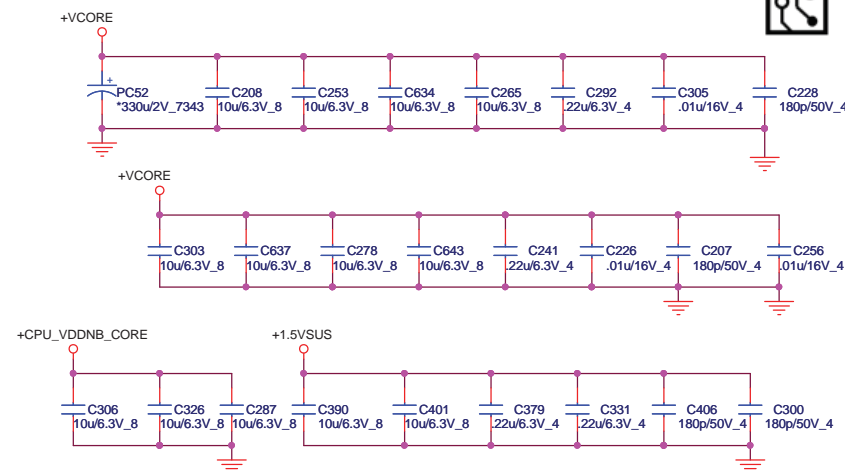


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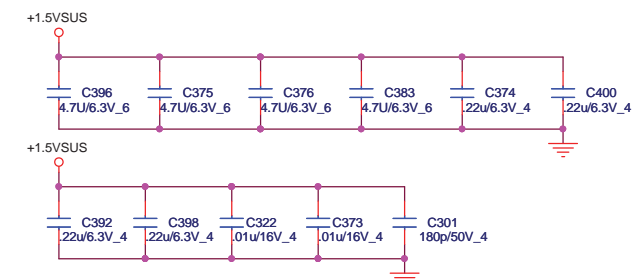
Size	Document Number	Rev
	Block Diagram	1A
Date: Monday, May 31, 2010	Sheet 1 of 48	



BOTTOM SIDE DECOUPLING



DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE



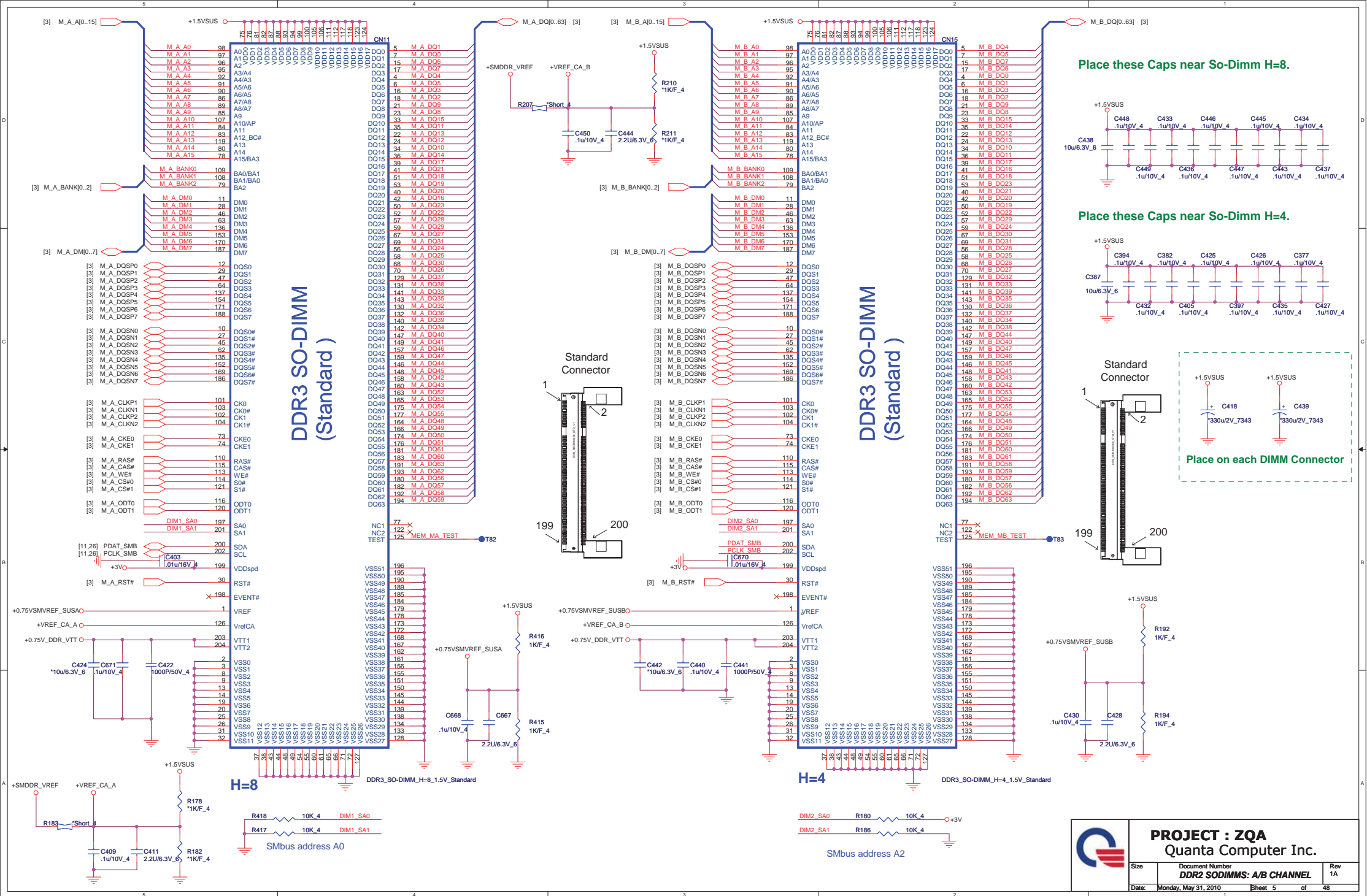
PROCESSOR POWER AND GROUND

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Size	Document Number S1G4 PWR & GND 3/3	Rev 1A
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Signals	RS880	RX880
HT_TXCALP	Ra 301 ohm 1%	Ra 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	Rb 301 ohm 1%	Rb 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

U16D		PAR 4 of 6	
AB12	MEM_A0(NC)	MEM_D0Q/DVO_VSYNC(NC)	AA18
AE16	MEM_A1(NC)	MEM_D0I1/DVO_HSYNC(NC)	AA20
X V11	MEM_A2(NC)	MEM_D02/DVO_DE(NC)	AA19
AE15	MEM_A3(NC)	MEM_D03/DVO_D0(NC)	Y19
AA12	MEM_A4(NC)	MEM_D04(NC)	Y17
AB16	MEM_A5(NC)	MEM_D05/DVO_D1(NC)	AA17
AD14	MEM_A6(NC)	MEM_D06/DVO_D2(NC)	AA15
AD13	MEM_A7(NC)	MEM_D07/DVO_D4(NC)	Y15
AD15	MEM_A8(NC)	MEM_D08/DVO_D3(NC)	AC20
AC18	MEM_A9(NC)	MEM_D09/DVO_D5(NC)	AD19
AE13	MEM_A10(NC)	MEM_DQ10/DVO_D6(NC)	AC18
AC14	MEM_A11(NC)	MEM_DQ11/DVO_D7(NC)	AB20
X Y14	MEM_A12(NC)	MEM_DQ12(NC)	AD22
	MEM_A13(NC)	MEM_DQ13/DVO_D9(NC)	AC22
AD18	MEM_BA0(NC)	MEM_DQ14/DVO_D10(NC)	AD21
AE17	MEM_BA1(NC)	MEM_DQ15/DVO_D11(NC)	
AD17	MEM_BA2(NC)		Y17
		MEM_DQS0P/DVO_IDCKP(NC)	W18
X W12	MEM_RASb(NC)	MEM_DQS0N/DVO_IDCKN(NC)	AD20
AD12	MEM_CASb(NC)	MEM_DQS1P(NC)	AE21
AB13	MEM_WEb(NC)	MEM_DQS1N(NC)	
AB18	MEM_Csb(NC)		W17
X Y14	MEM_Cke(NC)	MEM_DM0(NC)	AE19
	MEM_ODT(NC)	MEM_DM1/DVO_D8(NC)	
			AE23
X V15	MEM_CKP(NC)	IOPLLVD18(NC)	AE24
X W14	MEM_CKN(NC)	IOPLLVD1(NC)	
			AD23
AE12	MEM_COMPp(NC)	IOPLLVS(NC)	
AD12	MEM_COMPn(NC)	MEM_VREF(NC)	AE18

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Size	Document Number RS880M-HT LINK V/F 1/4	Rev 1A
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[15] PEG_RXP[15..0] ← PEG_RXP[15..0]
[15] PEG_RXN[15..0] ← PEG_RXN[15..0]

[15] PEG_TXP[15..0] ← PEG_TXP[15..0]
[15] PEG_TXN[15..0] ← PEG_TXN[15..0]

RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

U16B
PEG_RXP15 D4
PEG_RXN15 C4
PEG_RXP14 A3
PEG_RXN14 B3
PEG_RXP13 C2
PEG_RXN13 C1
PEG_RXP12 E5
PEG_RXN12 F5
PEG_RXP11 G5
PEG_RXN11 G6
PEG_RXP10 H5
PEG_RXN10 H6
PEG_RXP9 J6
PEG_RXN9 J5
PEG_RXP8 J7
PEG_RXN8 J8
PEG_RXP7 L5
PEG_RXN7 L6
PEG_RXP6 M8
PEG_RXN6 L8
PEG_RXP5 P7
PEG_RXN5 M7
PEG_RXP4 P5
PEG_RXN4 M5
PEG_RXP3 R8
PEG_RXN3 P8
PEG_RXP2 R6
PEG_RXN2 R5
PEG_RXP1 P4
PEG_RXN1 P3
PEG_RXP0 T4
PEG_RXN0 T3

PART 2 OF 6

PCIE I/F GFX

GFX_RX0P
GFX_RX0N
GFX_RX1P
GFX_RX1N
GFX_RX2P
GFX_RX2N
GFX_RX3P
GFX_RX3N
GFX_RX4P
GFX_RX4N
GFX_RX5P
GFX_RX5N
GFX_RX6P
GFX_RX6N
GFX_RX7P
GFX_RX7N
GFX_RX8P
GFX_RX8N
GFX_RX9P
GFX_RX9N
GFX_RX10P
GFX_RX10N
GFX_RX11P
GFX_RX11N
GFX_RX12P
GFX_RX12N
GFX_RX13P
GFX_RX13N
GFX_RX14P
GFX_RX14N
GFX_RX15P
GFX_RX15N

A5 PEG_TXP15 C C568
B5 PEG_TXN15 C C570
A4 PEG_TXP14 C C561
B4 PEG_TXN14 C C562
C3 PEG_TXP13 C C557
B2 PEG_TXN13 C C559
D1 PEG_TXP12 C C553
D2 PEG_TXN12 C C556
E2 PEG_TXP11 C C549
F1 PEG_TXN11 C C552
F4 PEG_TXP10 C C541
E3 PEG_TXN10 C C548
F1 PEG_TXP9 C C537
F2 PEG_TXN9 C C540
H4 PEG_TXP8 C C527
H3 PEG_TXN8 C C536
H1 PEG_TXP7 C C535
H2 PEG_TXN7 C C539
J2 PEG_TXP6 C C518
J1 PEG_TXN6 C C525
K4 PEG_TXP5 C C523
K3 PEG_TXN5 C C526
K1 PEG_TXP4 C C530
K2 PEG_TXN4 C C529
M4 PEG_TXP3 C C522
M3 PEG_TXN3 C C521
M1 PEG_TXP2 C C532
M2 PEG_TXN2 C C531
N2 PEG_TXP1 C C520
N1 PEG_TXN1 C C519
P1 PEG_TXP0 C C534
P2 PEG_TXN0 C C533

EV@.1u/10V 4 PEG_TXP15
EV@.1u/10V 4 PEG_TXN15
EV@.1u/10V 4 PEG_TXP14
EV@.1u/10V 4 PEG_TXN14
EV@.1u/10V 4 PEG_TXP13
EV@.1u/10V 4 PEG_TXN13
EV@.1u/10V 4 PEG_TXP12
EV@.1u/10V 4 PEG_TXN12
EV@.1u/10V 4 PEG_TXP11
EV@.1u/10V 4 PEG_TXN11
EV@.1u/10V 4 PEG_TXP10
EV@.1u/10V 4 PEG_TXN10
EV@.1u/10V 4 PEG_TXP9
EV@.1u/10V 4 PEG_TXN9
EV@.1u/10V 4 PEG_TXP8
EV@.1u/10V 4 PEG_TXN8
EV@.1u/10V 4 PEG_TXP7
EV@.1u/10V 4 PEG_TXN7
EV@.1u/10V 4 PEG_TXP6
EV@.1u/10V 4 PEG_TXN6
EV@.1u/10V 4 PEG_TXP5
EV@.1u/10V 4 PEG_TXN5
EV@.1u/10V 4 PEG_TXP4
EV@.1u/10V 4 PEG_TXN4
EV@.1u/10V 4 PEG_TXP3
EV@.1u/10V 4 PEG_TXN3
EV@.1u/10V 4 PEG_TXP2
EV@.1u/10V 4 PEG_TXN2
EV@.1u/10V 4 PEG_TXP1
EV@.1u/10V 4 PEG_TXN1
EV@.1u/10V 4 PEG_TXP0
EV@.1u/10V 4 PEG_TXN0

[24] PCIE_RX1+
[24] PCIE_RX1-

AE3
AD4
AE2
AD3

GPP_RX0P
GPP_RX0N
GPP_RX1P
GPP_RX1N

AE3
AD4
AE2
AD3

GPP_TX0P
GPP_TX0N
GPP_TX1P
GPP_TX1N

PCIE I/F GPP

GPP_RX2P
GPP_RX2N
GPP_RX3P
GPP_RX3N
GPP_RX4P
GPP_RX4N
GPP_RX5P
GPP_RX5N

AC1 PCIE_TXP0 C C546
AC2 PCIE_TXN0 C C545
AB4
AB3
AA2 PCIE_TXP2 C C543
AA1 PCIE_TXN2 C C544
Y1
Y2
Y4
Y3
V1
V2

.1u/10V 4
.1u/10V 4
.1u/10V 4
.1u/10V 4

PCIE_TX1+ [24]
PCIE_TX1- [24]
PCIE_TXP2 [26]
PCIE_TXN2 [26]

LAN

WLAN

[10] A_RXP0
[10] A_RXN0
[10] A_RXP1
[10] A_RXN1
[10] A_RXP2
[10] A_RXN2
[10] A_RXP3
[10] A_RXN3

AA8
Y8
AA7
Y7
AA5
AA6
W5
Y5

SB_RX0P
SB_RX0N
SB_RX1P
SB_RX1N
SB_RX2P
SB_RX2N
SB_RX3P
SB_RX3N

SB_TX0P
SB_TX0N
SB_TX1P
SB_TX1N
SB_TX2P
SB_TX2N
SB_TX3P
SB_TX3N

PCIE I/F SB

PCE_CALRP(PCE_BCALRP)
PCE_CALRN(PCE_BCALRN)

AD7 A_TXP0 C C573
AE7 A_TXN0 C C569
AE6 A_TXP1 C C560
AD6 A_TXN1 C C563
AB6 A_TXP2 C C555
AC6 A_TXN2 C C558
AD5 A_TXP3 C C547
AE5 A_TXN3 C C551

.1u/10V 4
.1u/10V 4
.1u/10V 4
.1u/10V 4
.1u/10V 4
.1u/10V 4
.1u/10V 4
.1u/10V 4

A_TXP0 [10]
A_TXN0 [10]
A_TXP1 [10]
A_TXN1 [10]
A_TXP2 [10]
A_TXN2 [10]
A_TXP3 [10]
A_TXN3 [10]

SB

AC8 NB_PCIECALRP R326 1.27K/F 4
AB8 NB_PCIECALRN R330 2K/F 4
+1.1V

INT HDMI

PEG_TXP15 C C76
PEG_TXN15 C C78
PEG_TXP14 C C73
PEG_TXN14 C C75
PEG_TXP13 C C68
PEG_TXN13 C C71
PEG_TXP12 C C64
PEG_TXN12 C C67

IV@.1u/10V 4
IV@.1u/10V 4
IV@.1u/10V 4
IV@.1u/10V 4
IV@.1u/10V 4
IV@.1u/10V 4
IV@.1u/10V 4
IV@.1u/10V 4

IV_TX2_HDMI+ [23]
IV_TX2_HDMI- [23]
IV_TX1_HDMI+ [23]
IV_TX1_HDMI- [23]
IV_TX0_HDMI+ [23]
IV_TX0_HDMI- [23]
IV_TXC_HDMI- [23]

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For Check list JTAG



For A11 version

(02/10) Don't need 49.9 ohm PD.



STRAP_DEBUG_BUS_GPIO_ENABLEB

Enables the Test Debug Bus using GPIO.

RS880M	
1 Disable	V
0 Enable	



RS880M: Enables Side port memory

RS880M:INT_CRT_HSYNC

Selects if Memory SIDE PORT is available or not

1 = Memory Side port Not available

0 = Memory Side port available

Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

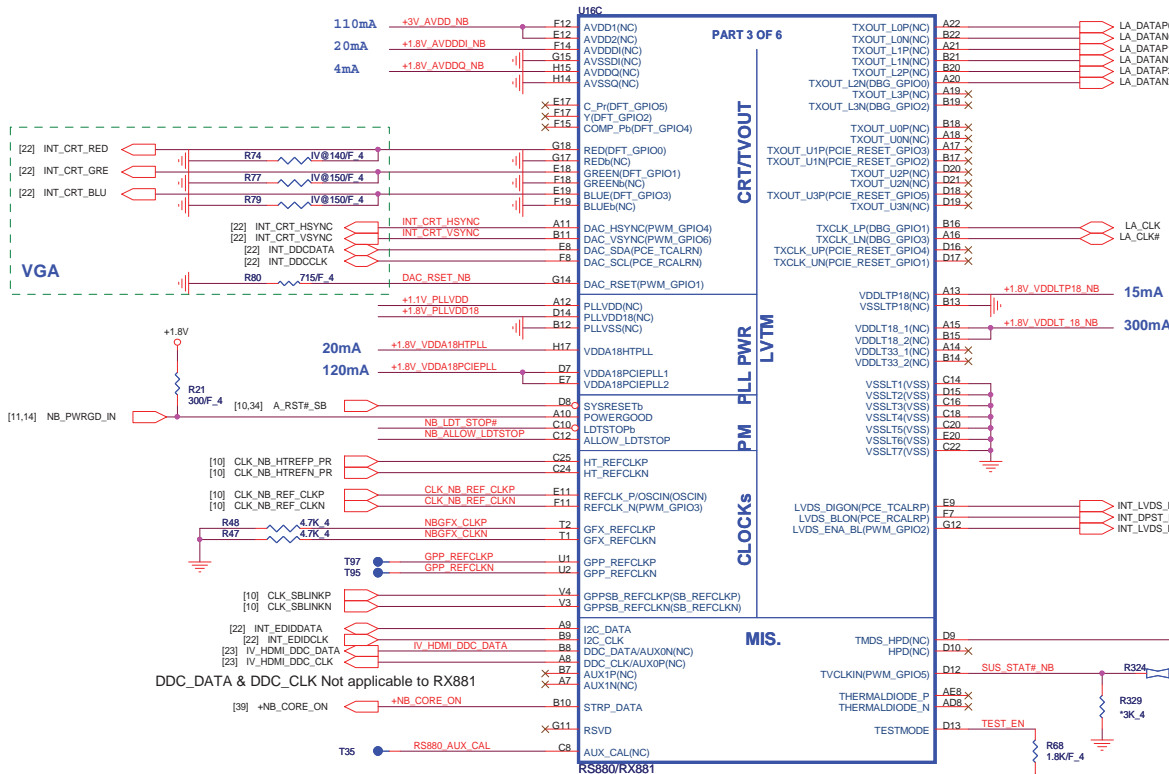


For external EEPROM Debug only

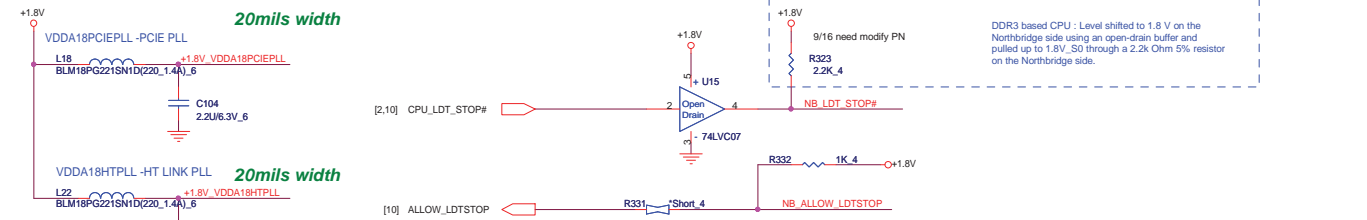
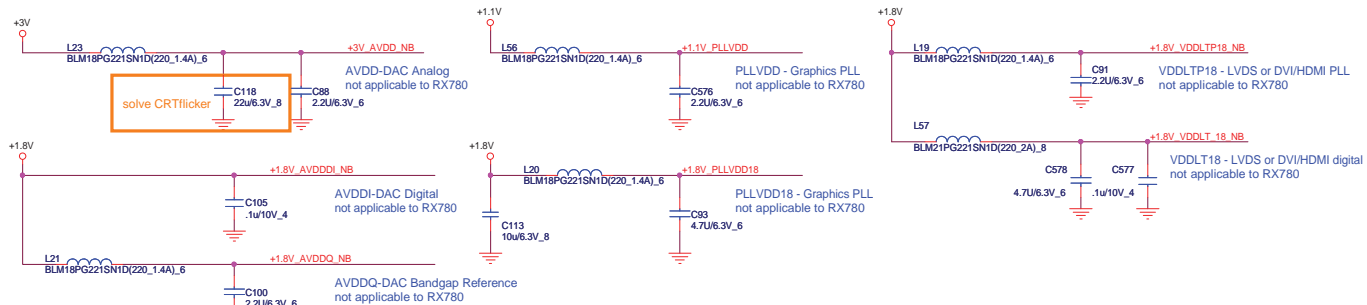
RS780/RX780/RS880



Display Port interface from PCIeGraphics (RS880/rs880M only)



RS880M --- ADD



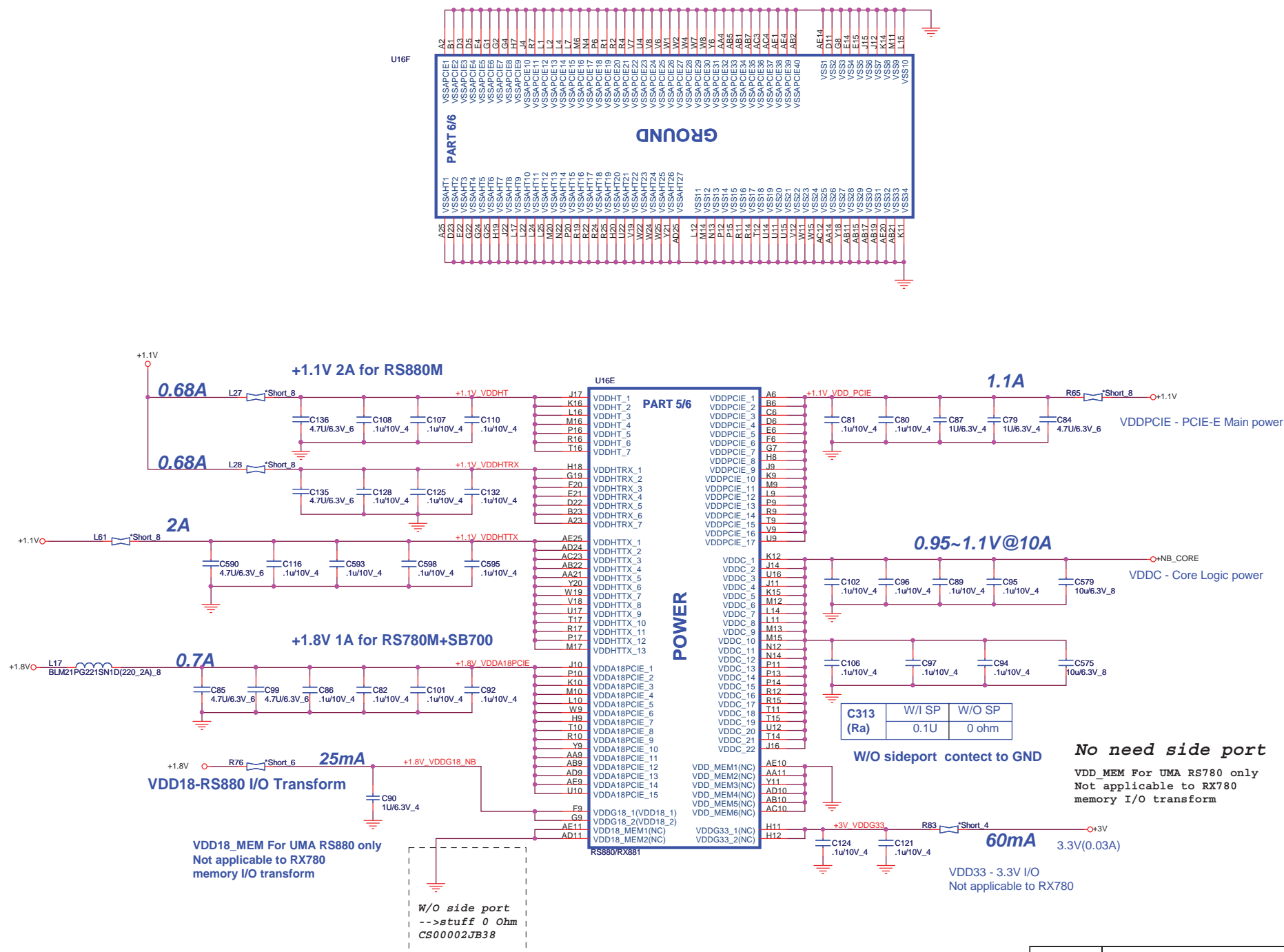
<http://hobi-elektronika.net>

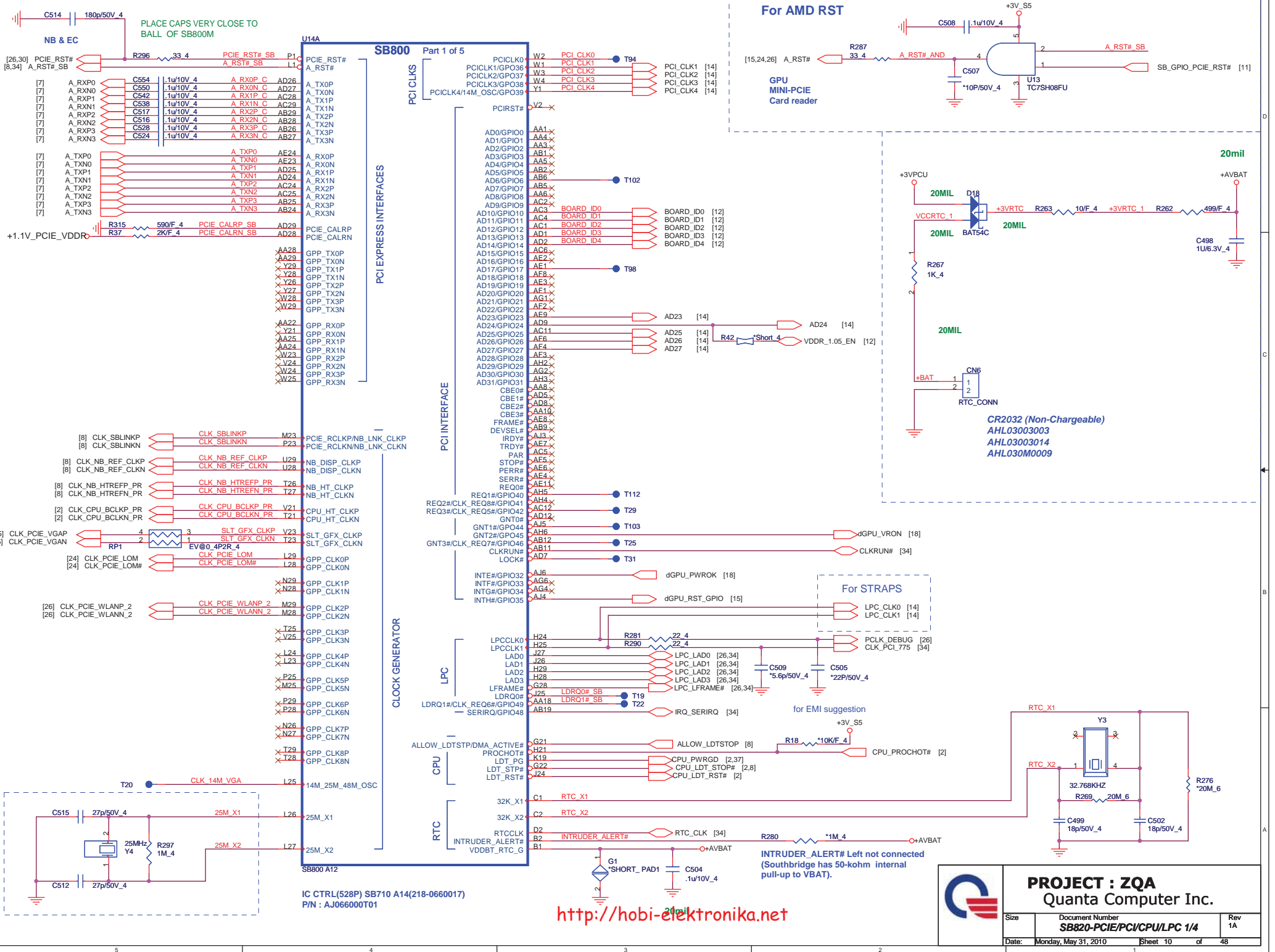
The LDTREC# connection from the CPU to ALLOW_LDTSTOP of the Northbridge is no longer required.



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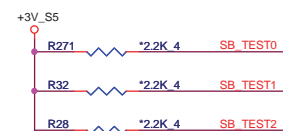
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NC only .Can't be install

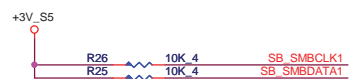


SCL0/SDATA0 is 3V tolerance. AMD datasheet define it

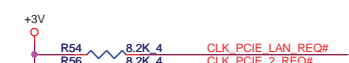
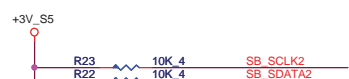
Clk Gen/ Robson/ TV tuner/ DDR2/ Thermal/ Accelerometer



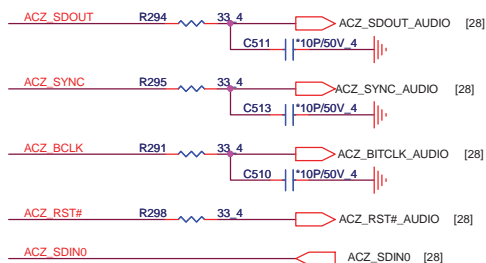
SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it



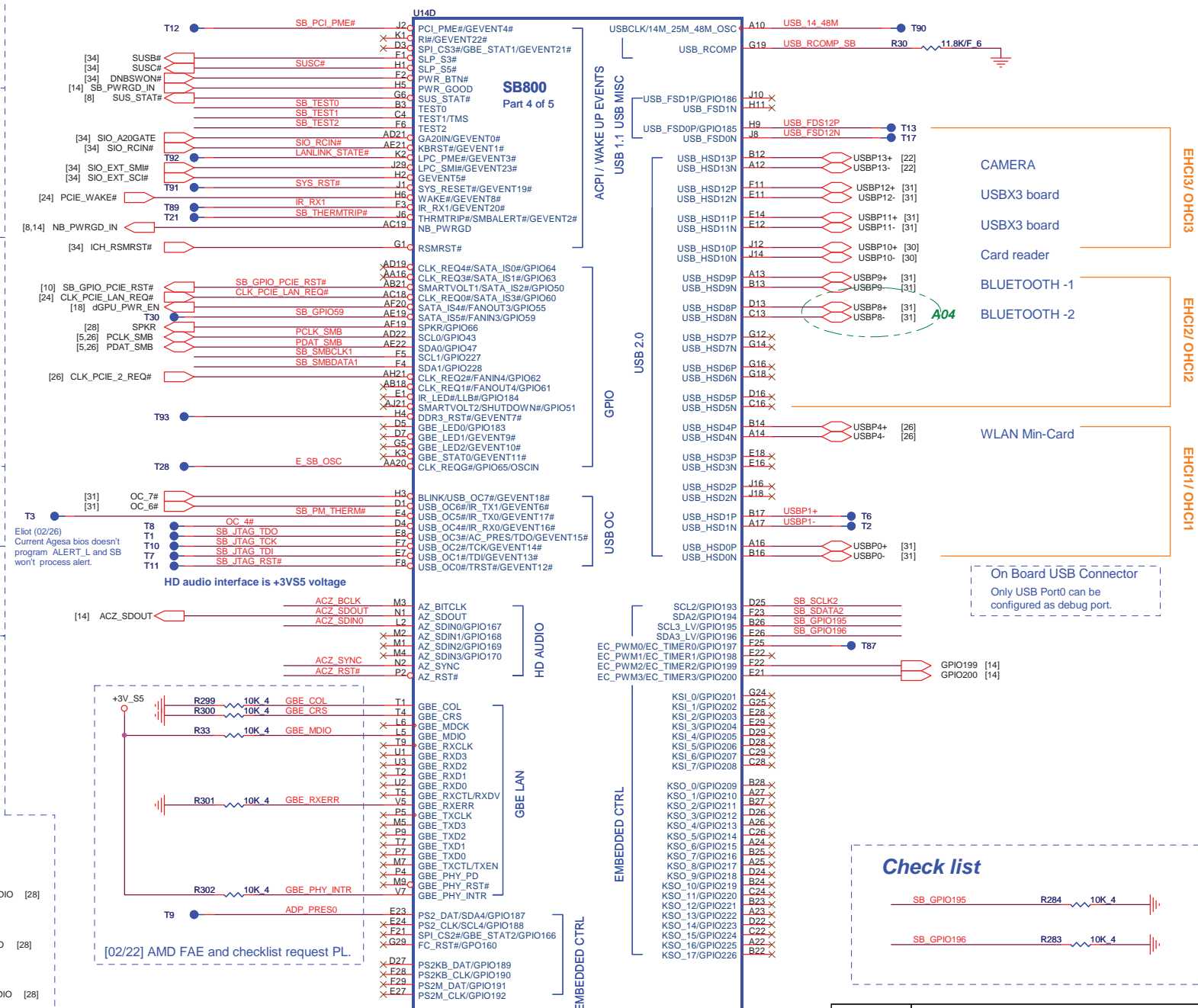
SCL2/SDATA2 is 3V/S5 tolerance.
AMD datasheet define it



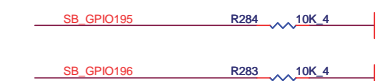
To Azalia



USBCLK/41M_25M_48M_OSC pin is CLK input pin when EXT CLKGEN mode.
It is output CLK source when INT CLKGEN mode.



Check list



PROJECT : ZQA
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Size	Document Number SB820-ACPI/GPIO/USB 2/4	Rev 1A
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[27]	SATA_TX0+	C567	.01u16V 4	SATA TX0+ - C
[27]	SATA_TX0-	C566	.01u16V 4	SATA TX0- - C
[27]	SATA_RX0-			
[27]	SATA_RX0+			
[27]	SATA_TX1+	C565	.01u16V 4	SATA TX1+ - C
[27]	SATA_TX1-	C564	.01u16V 4	SATA TX1- - C
[27]	SATA_RX1-			
[27]	SATA_RX1+			

SATA PORT 0,1,2,3 can support AHCI mode

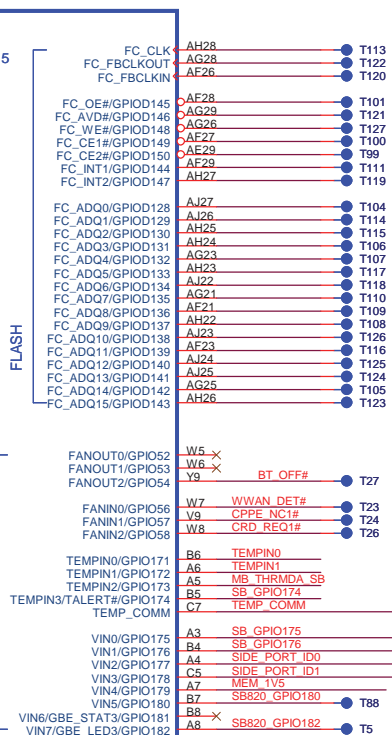
Signal Name	Explanation
SATA_CALRP	SB800 A11: 800 ohm 1% resistor to GND. SB800 A12: 1K ohm 1% resistor to GND.
SATA_CALRN	SB800 A11: 931 ohm 1% resistor to VDDAN_11_SATA. SB800 A12: 931 ohm 1% resistor to VDDAN_11_SATA.

The schematic diagram illustrates the SATA interface circuit. It shows the connection of the SATA controller pins to the SATA connector. The +1.1V_AVDD_SATA pin is connected to the SATA_CALRP pin via a 1K/4 resistor (R39) and a 931F/4 capacitor (R40). The SATA_ACT# pin is connected to the AD11 pin via a 3V0 voltage source and a 52 resistor (R52). The SATA_X1 and SATA_X2 pins are connected to the AD16 and AC16 pins via 27pF capacitors (C572, C571) and 50V_4 capacitors. The SATA_X1 and SATA_X2 pins are also connected to the AD16 and AC16 pins via 25M/4 capacitors (Y5) and 1M_4 capacitors (R322). The SATA_X1 and SATA_X2 pins are also connected to the AD16 and AC16 pins via 27pF capacitors (C572, C571). The SATA_X1 and SATA_X2 pins are also connected to the AD16 and AC16 pins via 27pF capacitors (C572, C571).

PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820

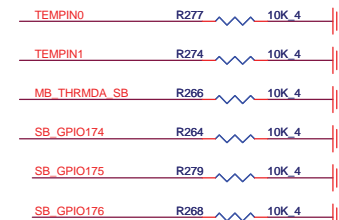


Part 2 of 5

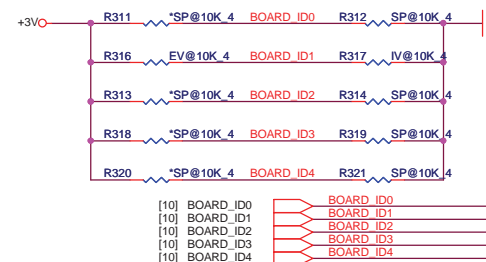


IF THERE IS NO IDE, TEST POINTS FOR
DEBUG BUS IS MANDATORY

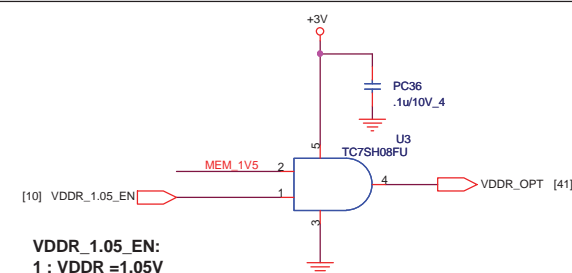
Check list



BOM check



	1	0
ID0		
ID1	DIS	UM
ID2		
ID3		
ID4		



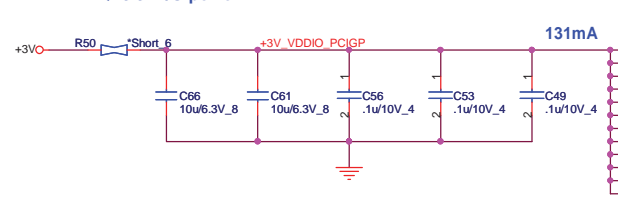
VDDR_1.05_EN:
1 : VDDR =1.05V
0 : VDDR = 0.9V (Default)



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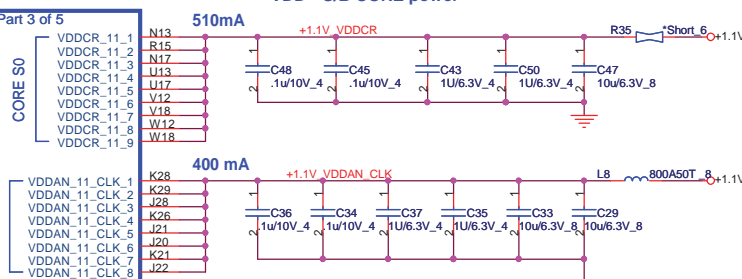
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VDDQ--3.3V I/O power

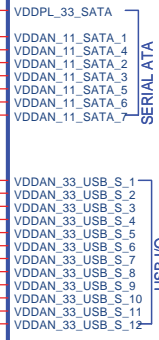
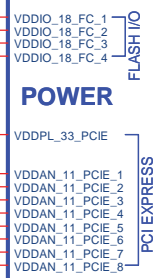
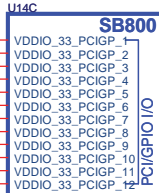
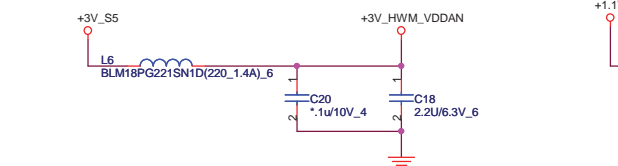
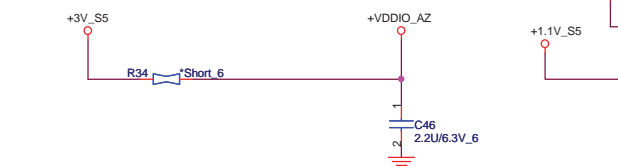
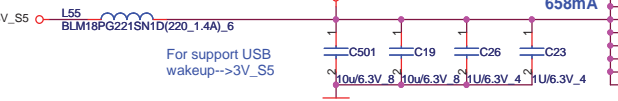
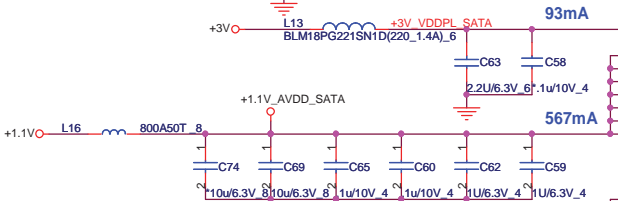
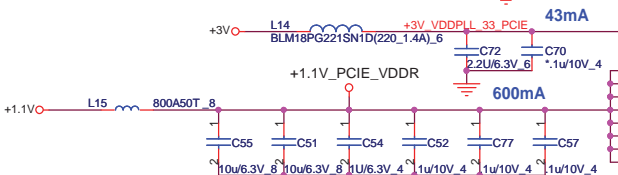


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

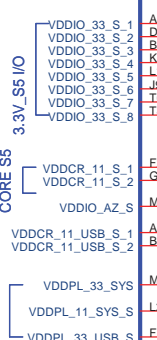
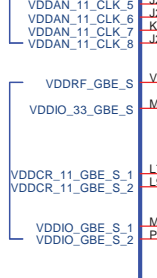
VDD-- S/B CORE power



POWER

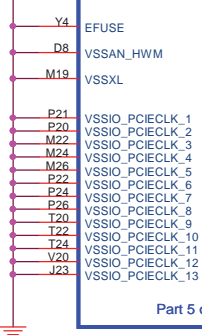
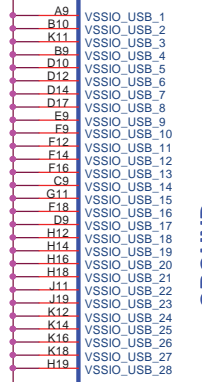
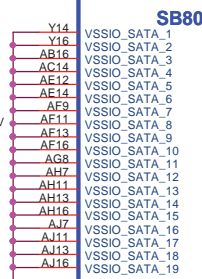
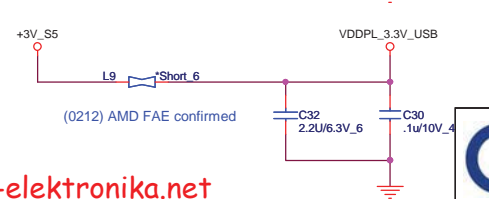
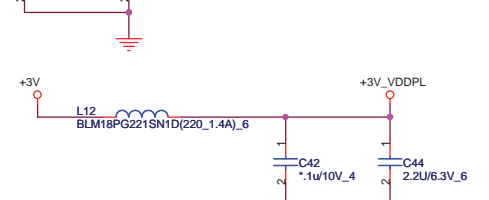
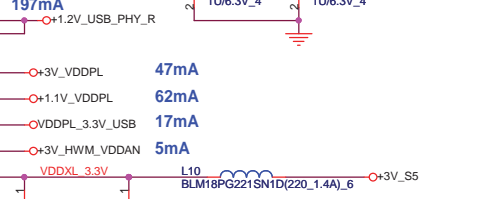
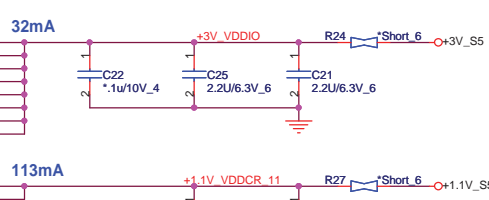


SB800 A12



SB800 A12

SB820 without GBE/ Connected to GND plane.



SB800 A12

GROUND

Part 5 of 5

<http://hobi-elektronika.net>



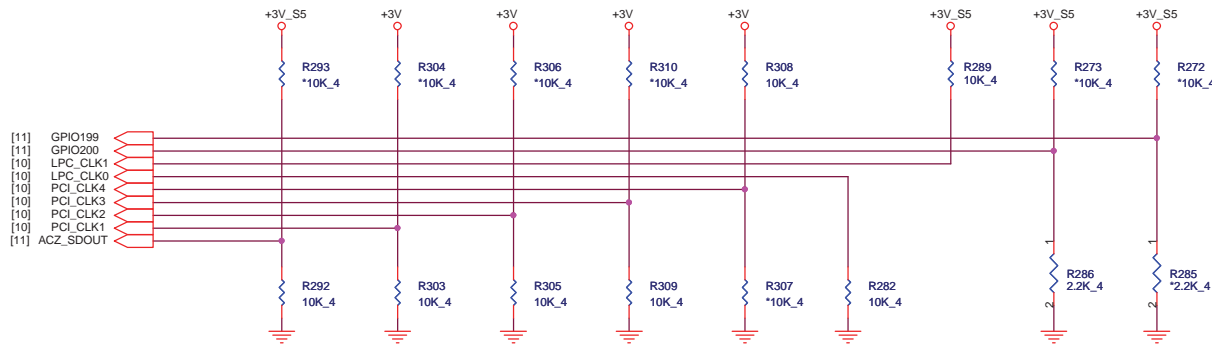
PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	SB820-PWR/DECOUPLING 4/4	1A
Date:	Monday, May 31, 2010	Sheet 13 of 48

REQUIRED STRAPS

SB820M is supported Gen.1 mode only.

For internal clock GEN.

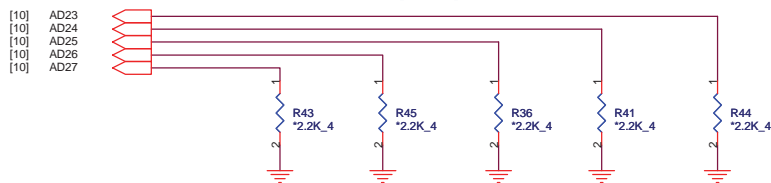


	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L, H=LPC ROM L, L=FWH ROM	DEFAULT

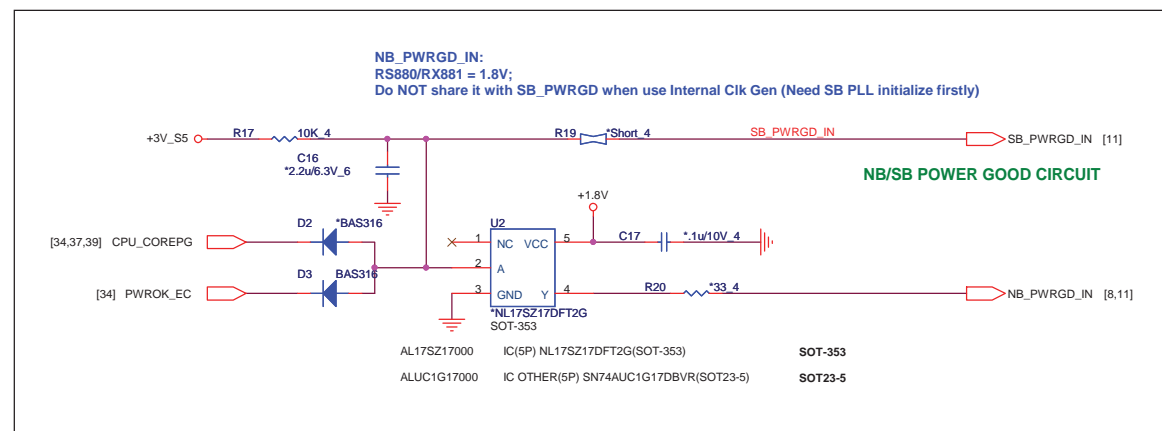
internal have pull Hi 10K

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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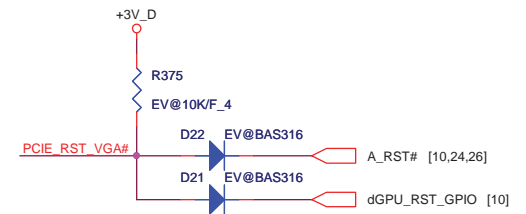
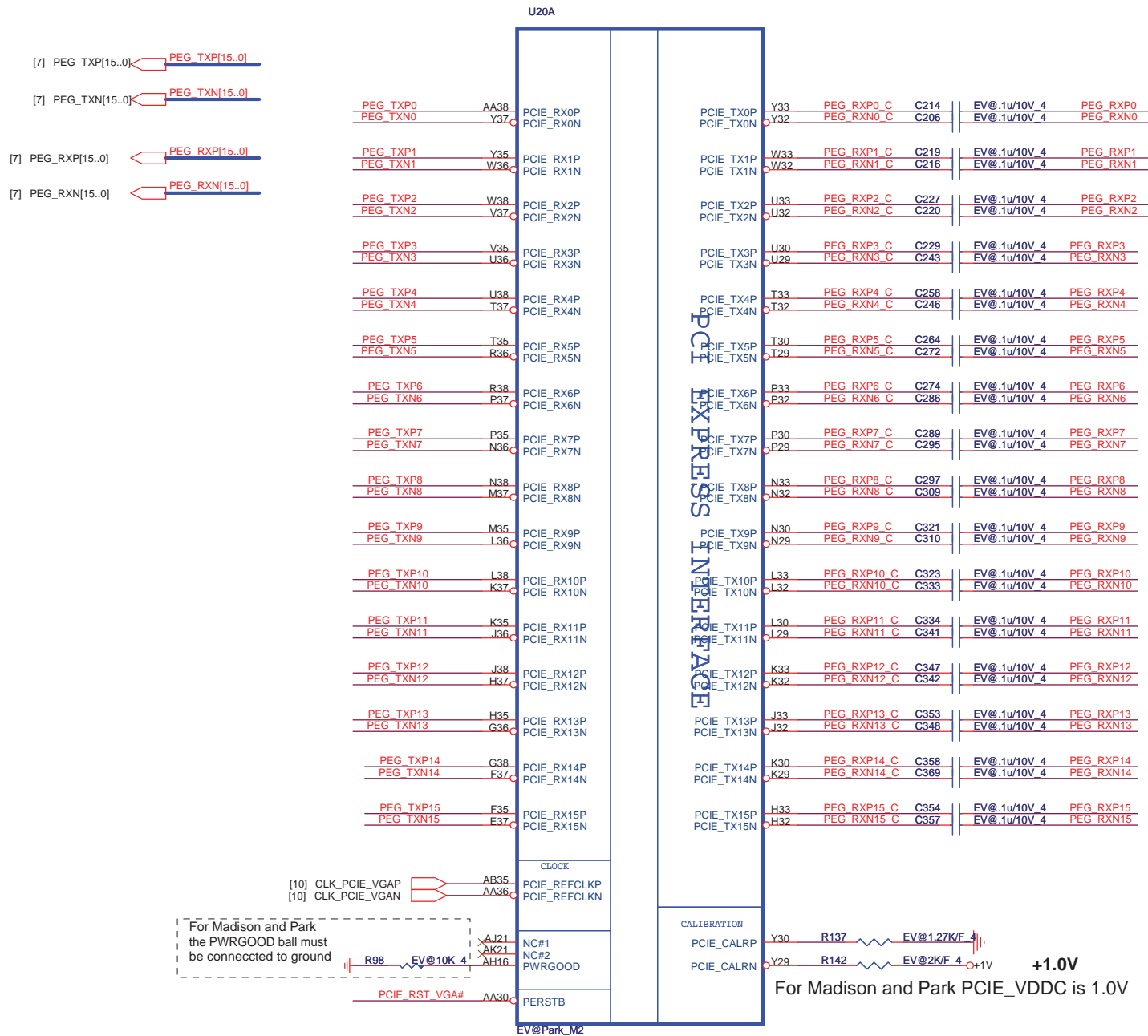
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

14



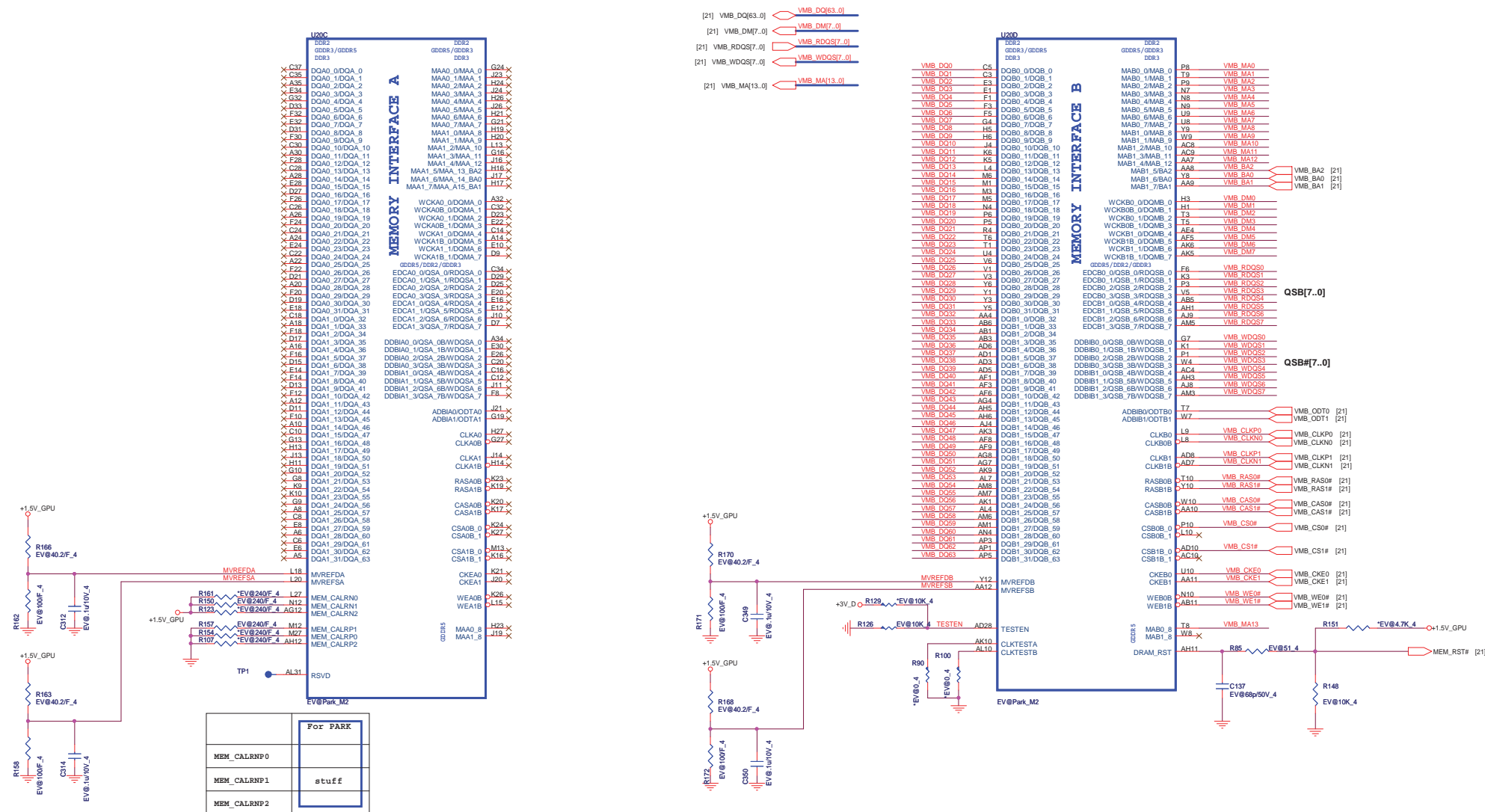
PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number SB820-STRAPS	Rev 1A
Date: Monday, May 31, 2010	Sheet 14	of 48



PROJECT : ZQA
Quanta Computer Inc.

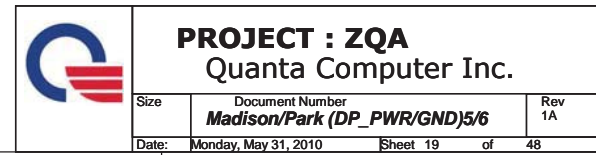
Size	Document Number	Rev
	Madison/Park-PCIE 1/6	1A
Date:	Monday, May 31, 2010	Sheet 15 of 48



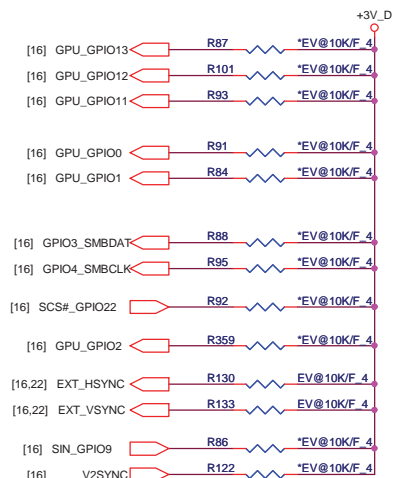
DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R





PIN STRAPS



Memory Aperture size

GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

ROM Table

EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

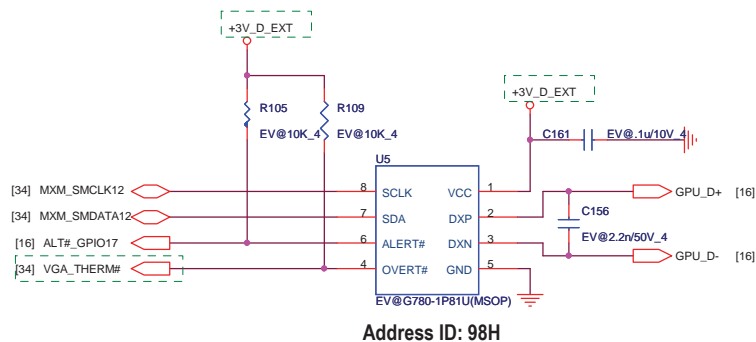
20

DDR3 Memory Aperture size

DDR3 Memory Aperture size

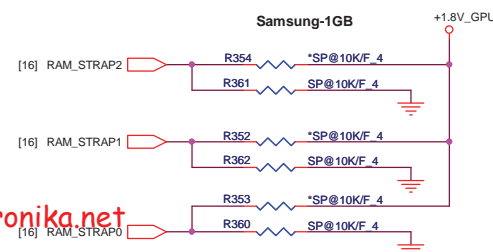
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVDPDATA_2	RAM_STRAP1 DVDPDATA_1	RAM_STRAP0 DVDPDATA_0
Hynix			512MB	1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB	1	0	0
			2GB	1	1	1
Samsung			512MB	0	1	0
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1

Thermal Sensor



Address ID: 98H

<http://hobi-elektronika.net>

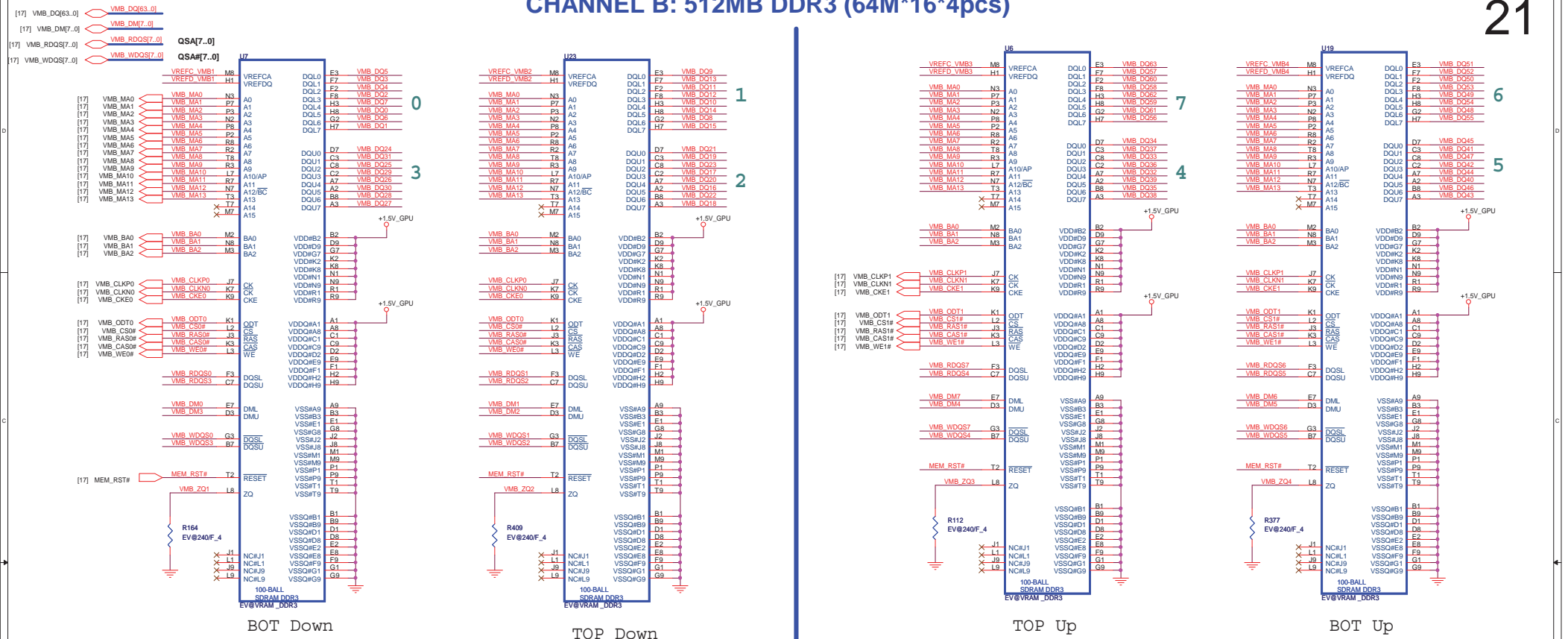


RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

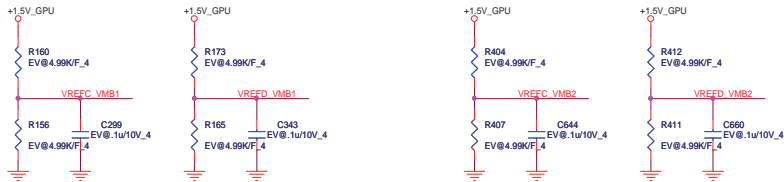
			PROJECT : ZQA Quanta Computer Inc.		
Size	Document Number				Rev 1A
Medison/Park Strip/Thermal 6/6				Date:	Monday, May 31, 2010
				Sheet	20 of 48

CHANNEL B: 512MB DDR3 (64M*16*4pcs)

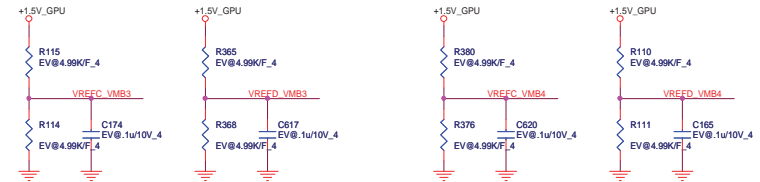
21



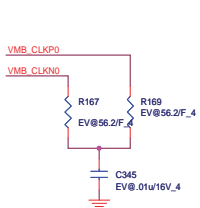
Group-B0 VREF



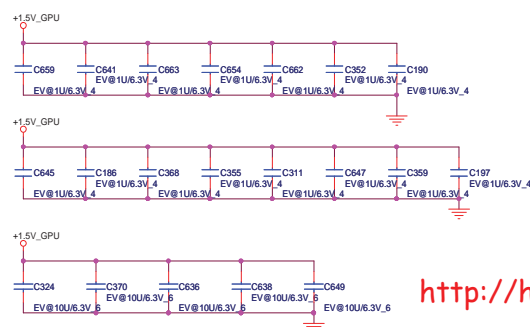
Group-B1 VREF



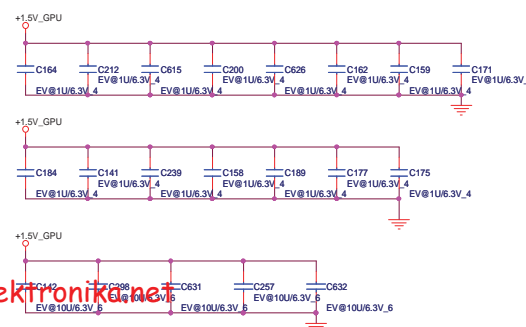
MEM_B0 CLK



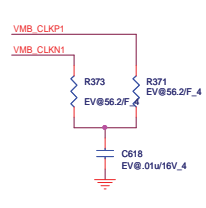
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



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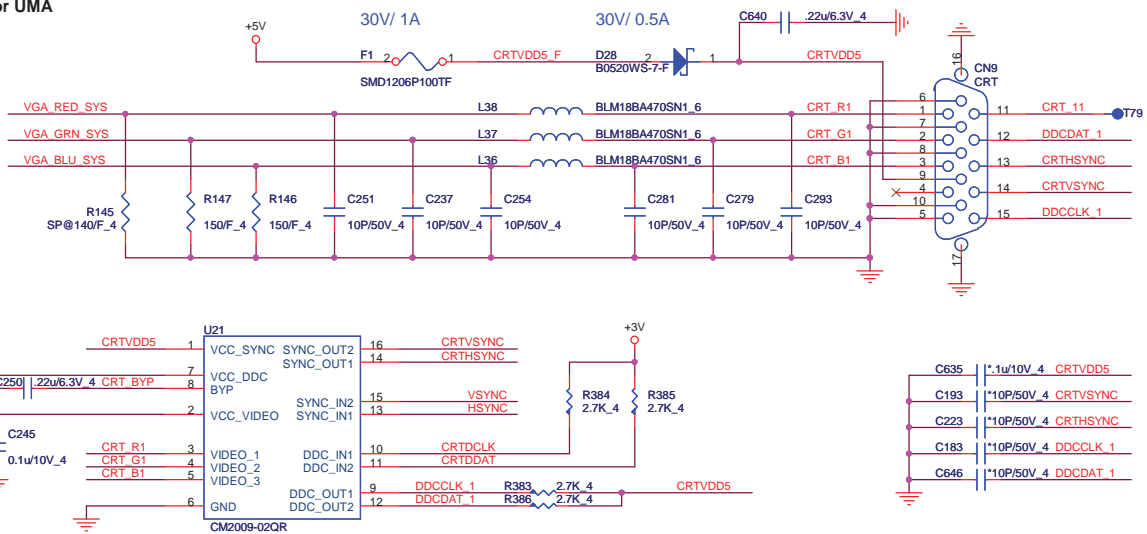
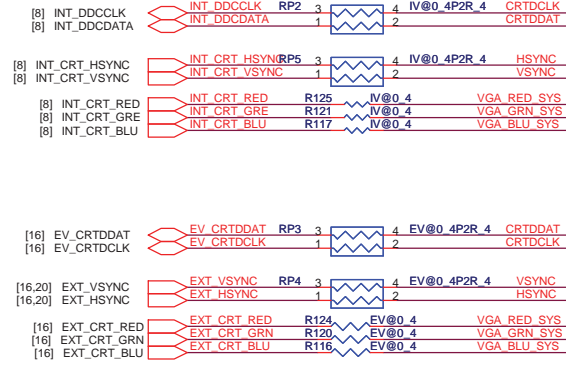
PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	MEMORY 2 channel B	1A
Date:	Monday, May 31, 2010	Sheet 21 of 48

CRT

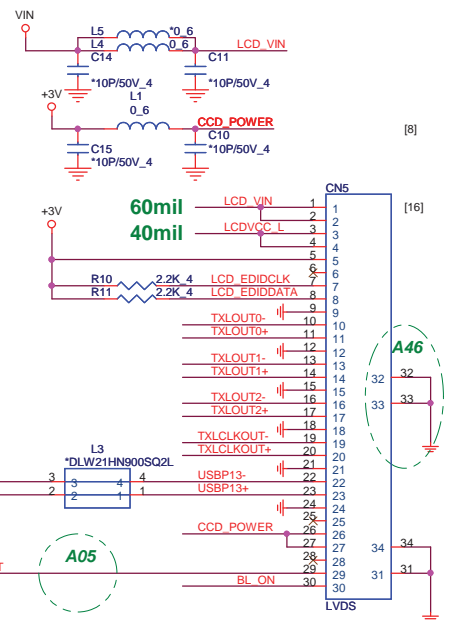
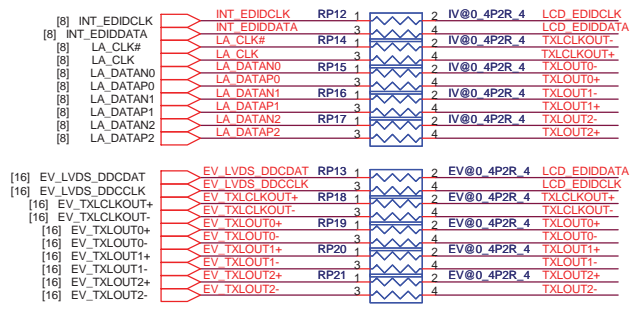
OPTION SIGNAL FROM NB to LVDS/CRT for UMA

OPTION SIGNAL FROM NB to CRT for UMA

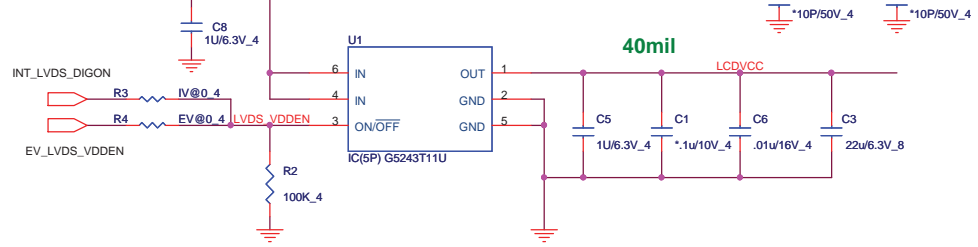


OPTION LCDVCC SIGNAL FROM NB to LVDS for UMA

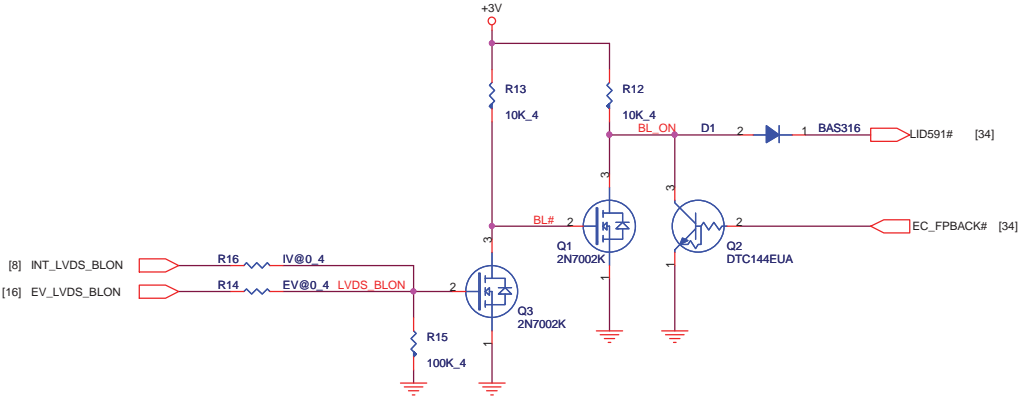
LVDS(LDS) OPTION SIGNAL FROM NB to LVDS for UMA



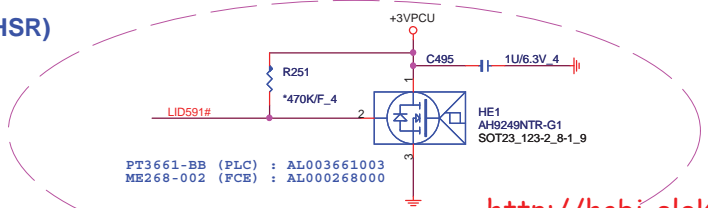
LCD PW(LDS)



Backlight Control(LDS)



Lid Switch (HSR)



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PROJECT : ZQA
Quanta Computer Inc.

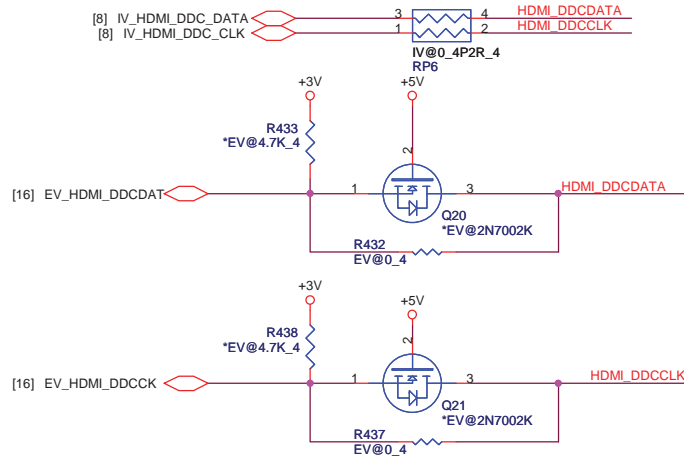
Size	Document Number CRT/LVDS/LID	Rev 1A
Date: Monday, May 31, 2010	Sheet 22 of 48	

HDMI SDVO I2C Control

UMA

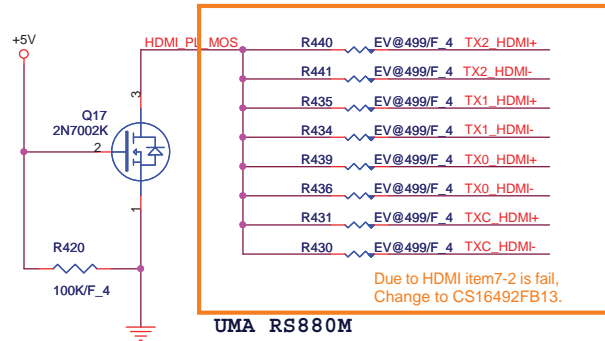
Close to HDMI Connector

DIS



HDMI (HDM)

Close to HDMI Connector



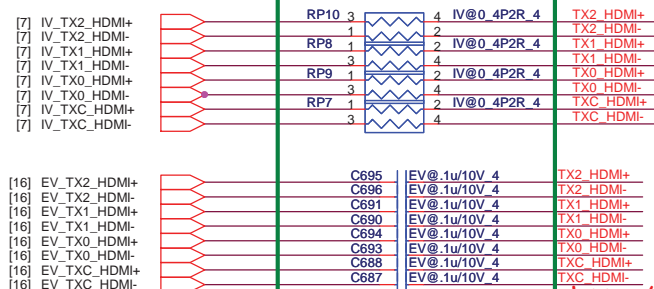
UMA RS880M

Stuff 715 ohm CS17152FB17

DIS Park-M2

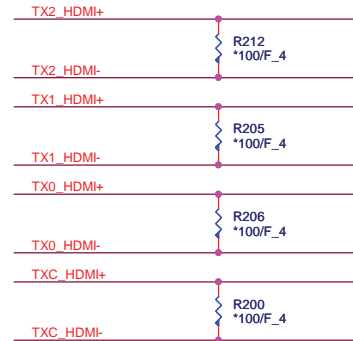
Stuff 499 ohm CS14992FB24

for Layout concern
,placement close HDMI conn

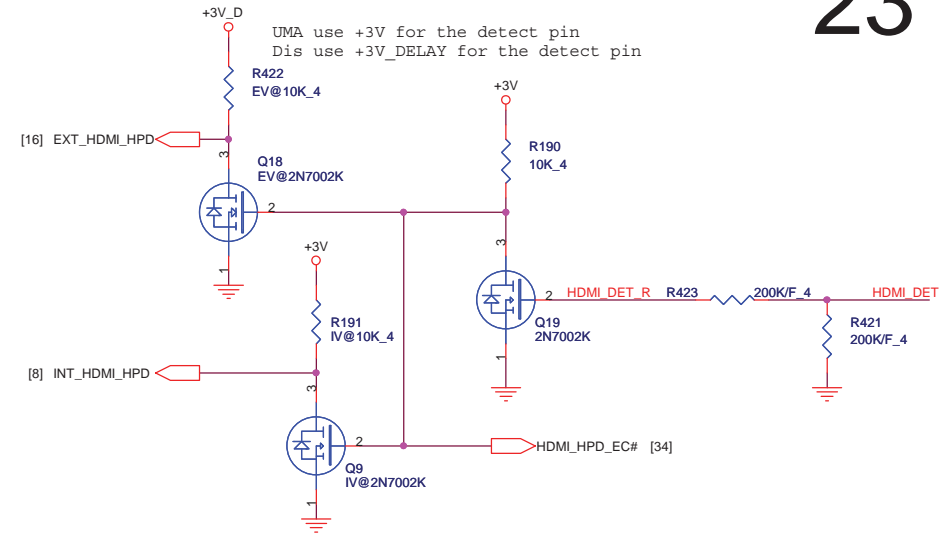


EMI reserve for HDMI(EMC)

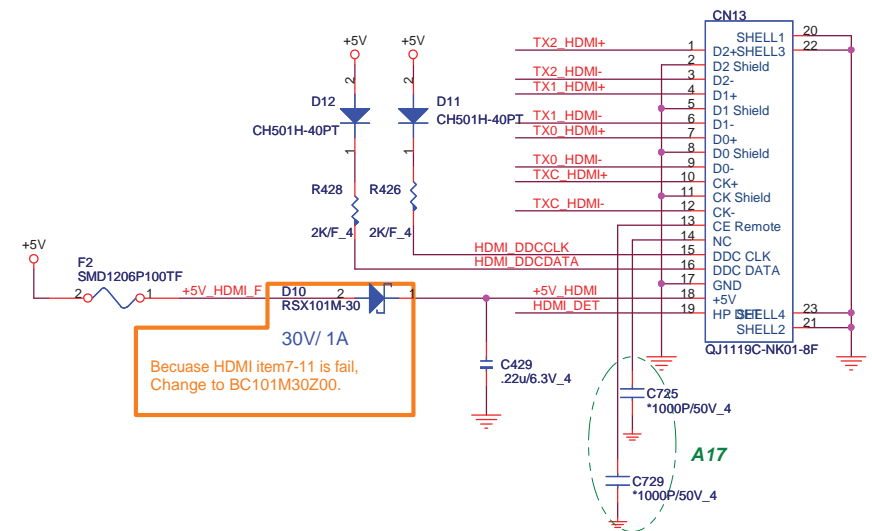
Close connector



HDMI HPD SENSE (HDM)



HDMI PORT (HDM)



PROJECT : ZQA
Quanta Computer Inc.

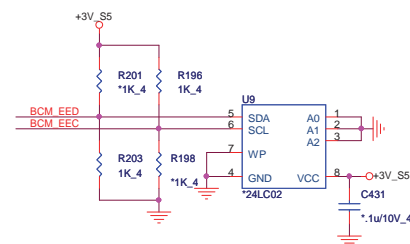
Size	Document Number	Rev
	HDMI	1A
Date:	Monday, May 31, 2010	Sheet 23 of 48

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23



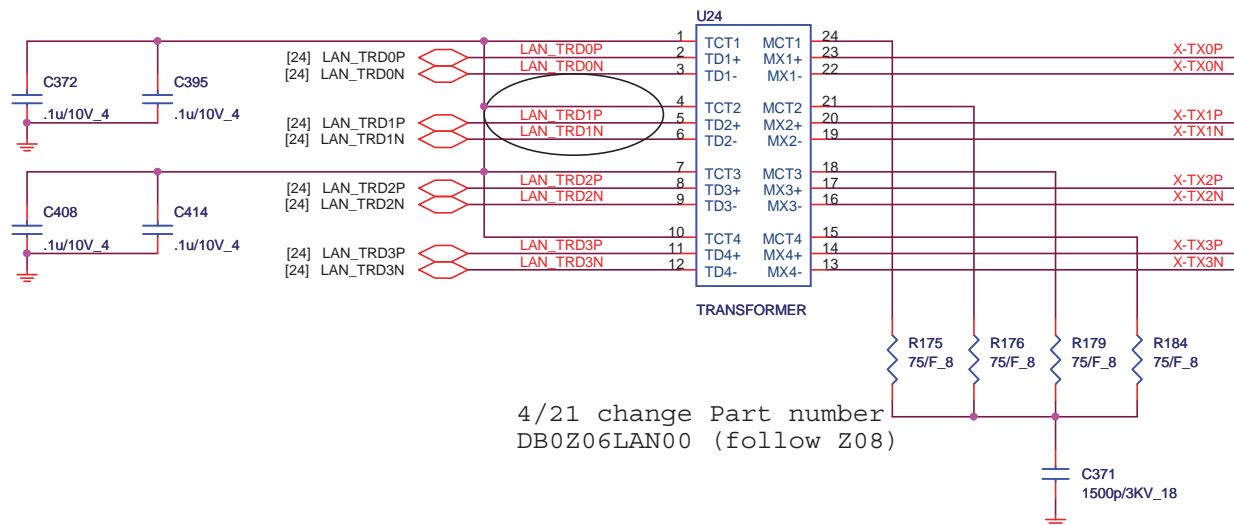
EEPROM



EEPROM Type	EECLK	EEDAT
24LC02	1	1
Internal	1	0

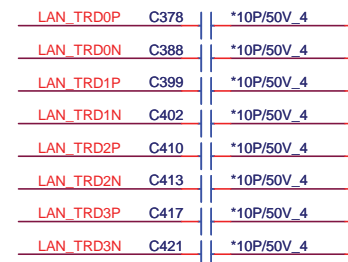
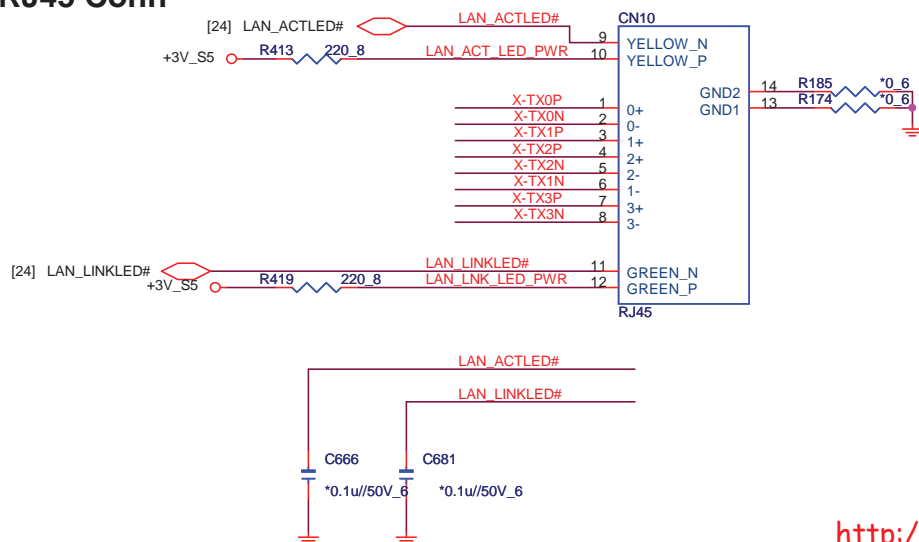
TRANSFORMER

4/27 modify it



For EMI

RJ45 Conn


<http://hobi-elektronika.net>

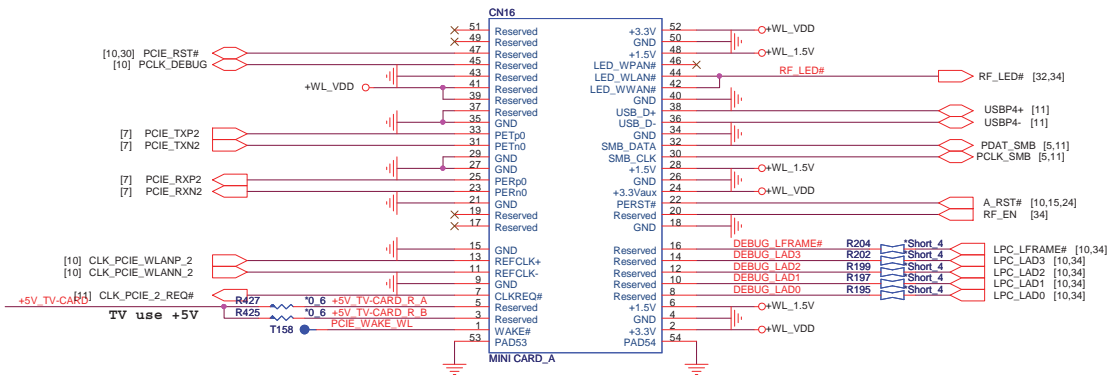

PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	LAN Transformer and RJ45	1A
Date:	Monday, May 31, 2010	Sheet 25 of 48

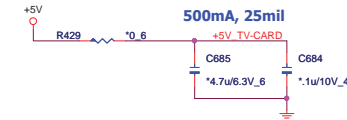
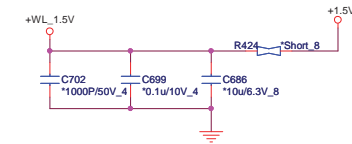
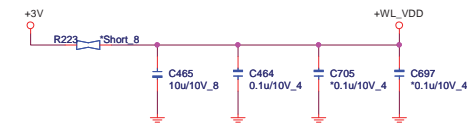
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

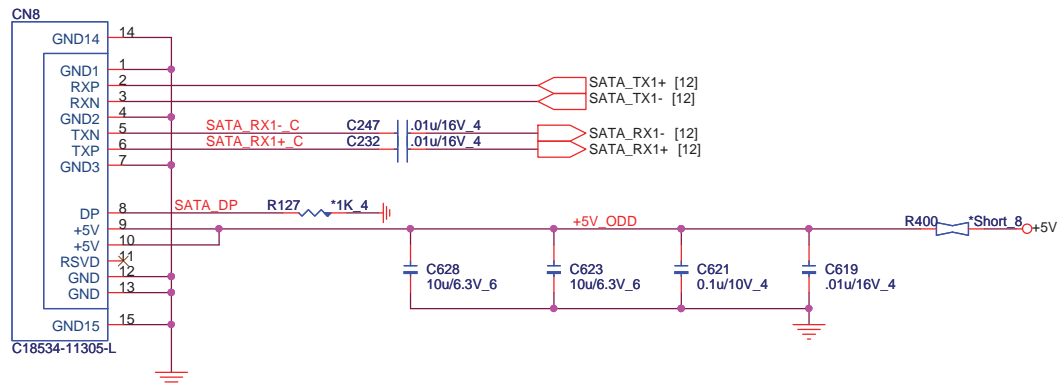
Check LED signal. (active high or low)



Debug



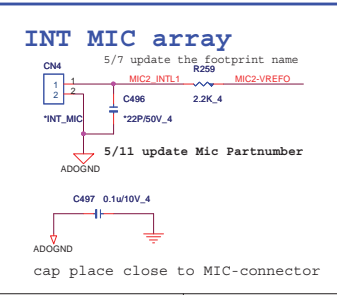
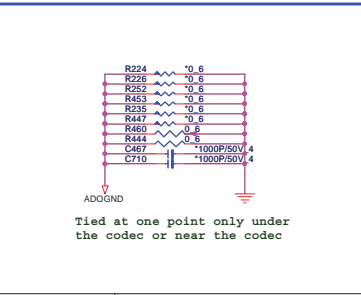
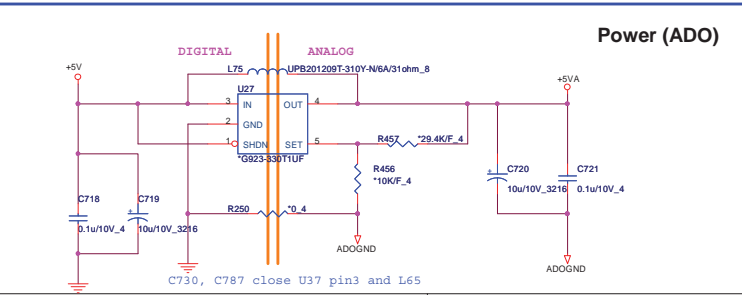
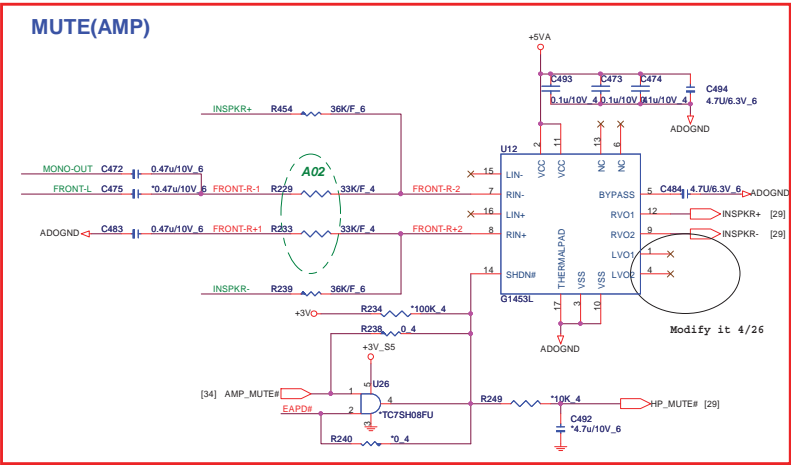
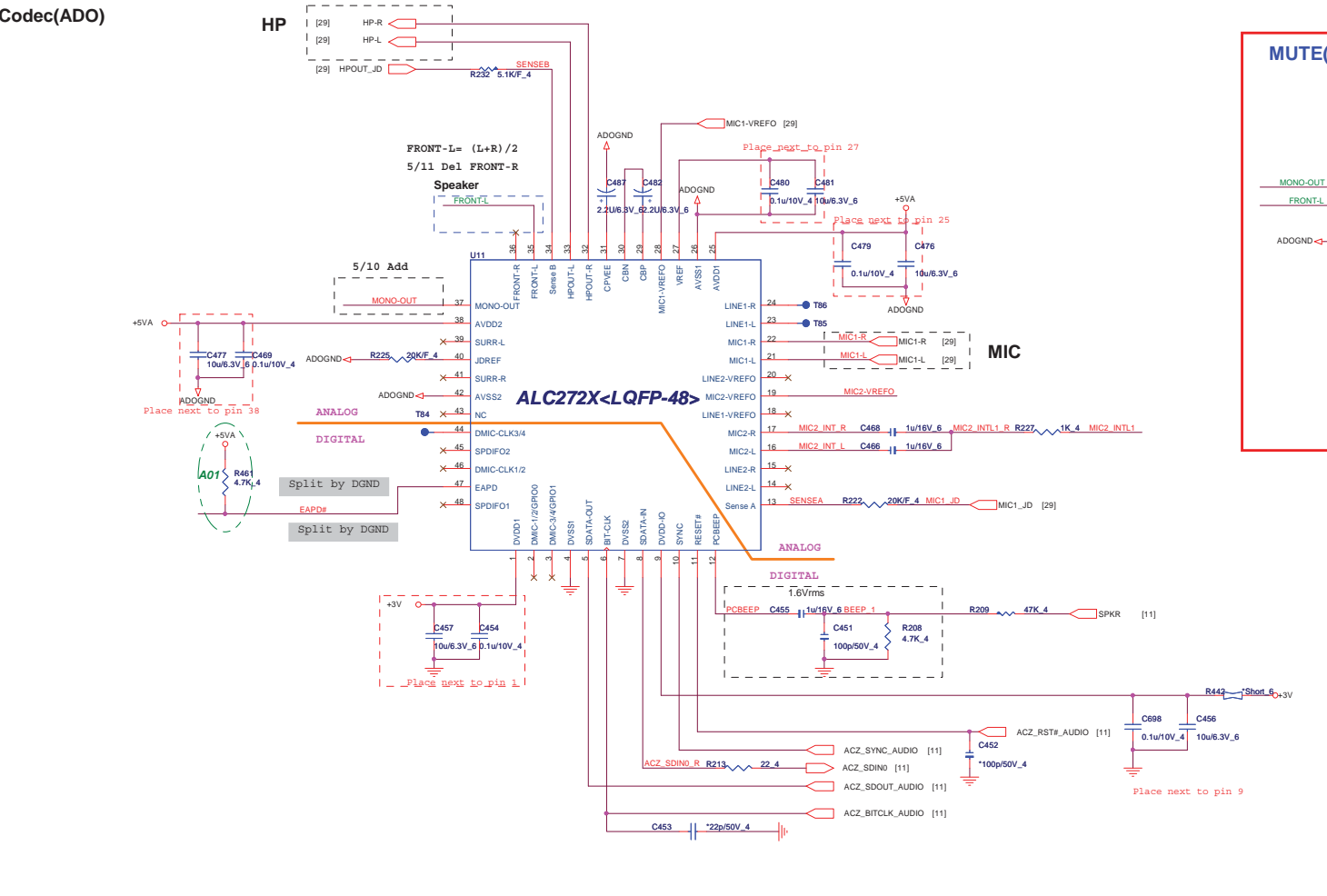
26




PROJECT : ZQA
Quanta Computer Inc.

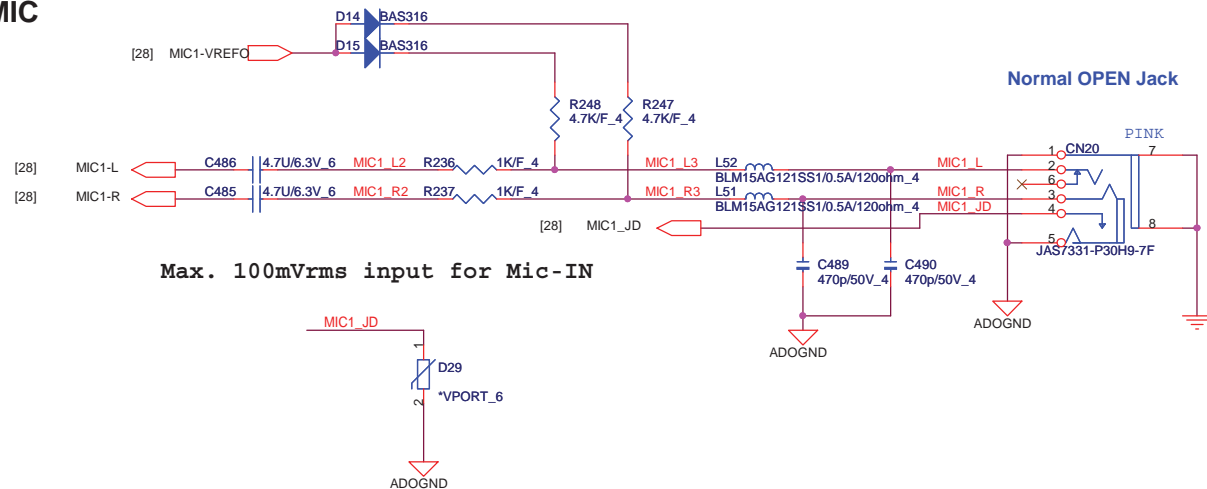
Size	Document Number SATA-HDD/ODD/HOLE	Rev 1A
Date:	Monday, May 31, 2010	Sheet 27 of 48

Codec(ADO)

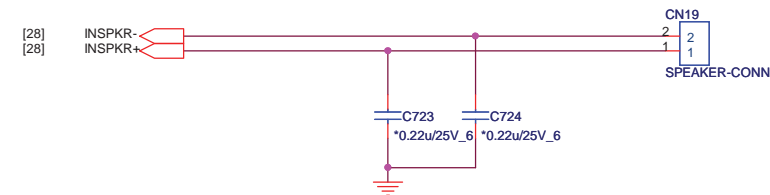


			
PROJECT : ZQA Quanta Computer Inc.			
Size	Document Number	Rev	
	REALTEK ALC663&888/MDC	1A	
Date:	Monday, May 31, 2010	Sheet	28 of 48

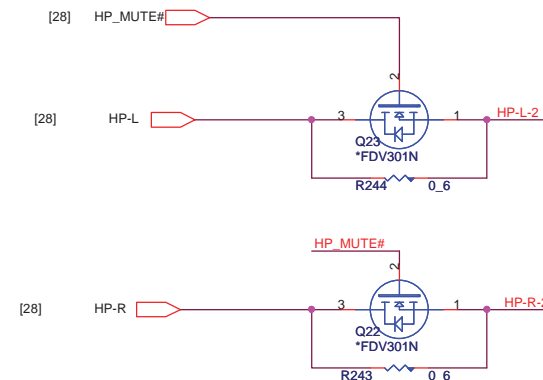
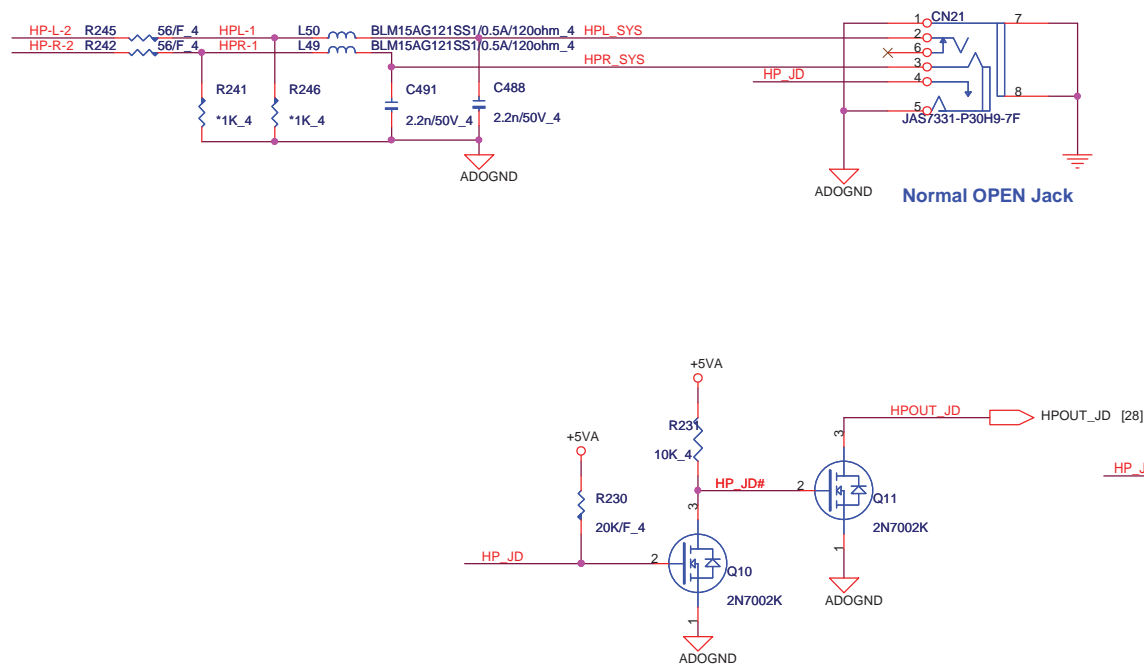
MIC




Internal Speaker



HP



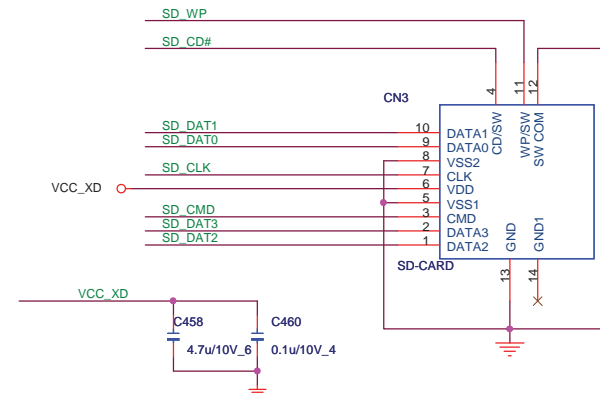
 PROJECT : ZQA Quanta Computer Inc.		
Size	Document Number AMP /AUDIO JACK CONN	Rev 1A
Date:	Monday, May 31, 2010	Sheet 29 of 48

CARD READER Controller

2 IN 1 CARD READER (MMC)

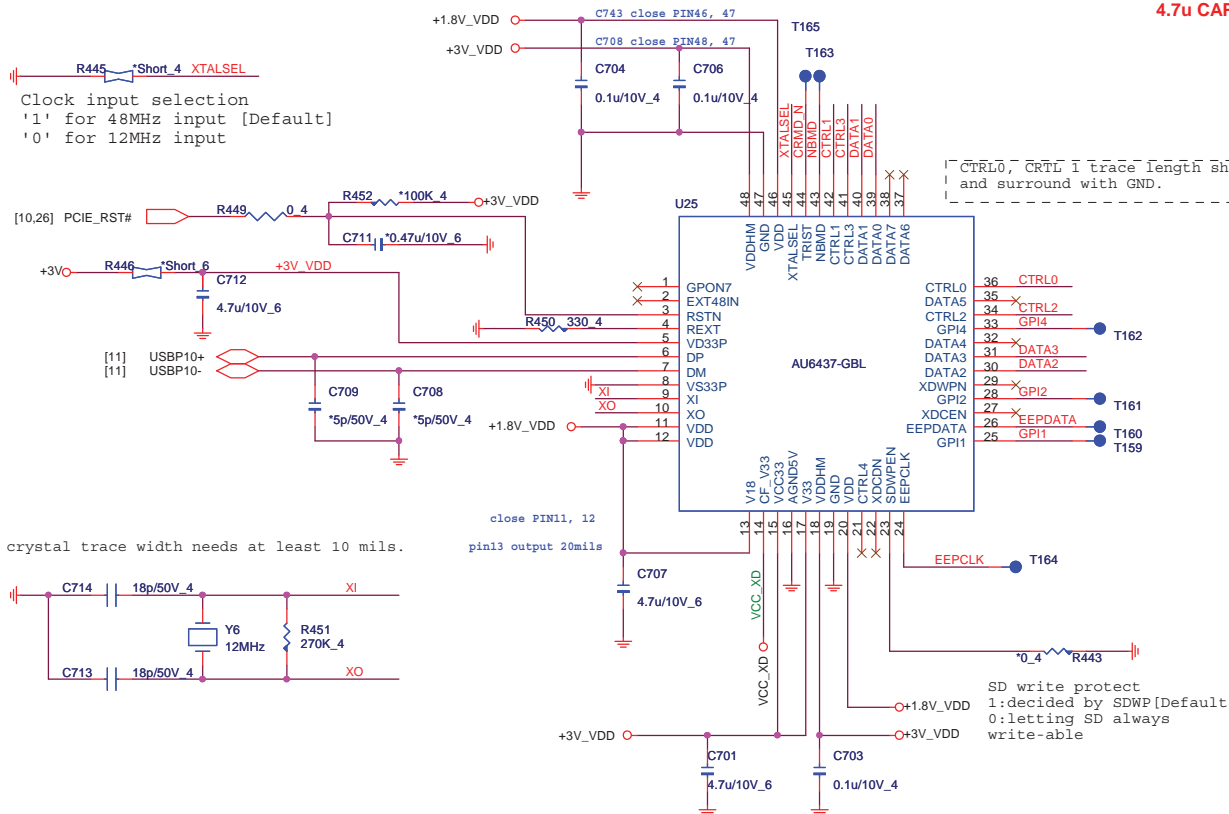
30

Main	DFHS11FR011
Second	DFHS11FR033

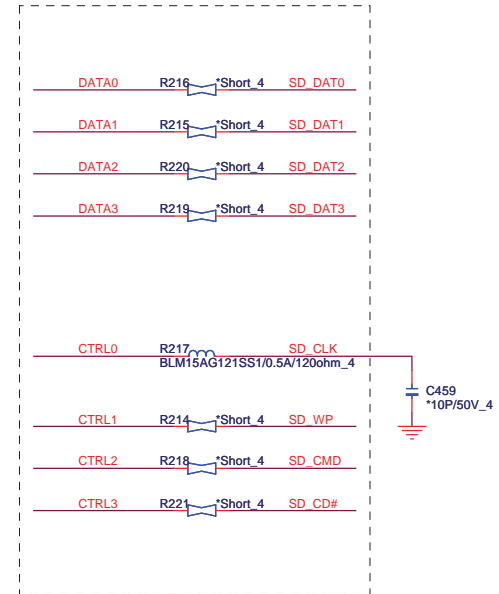


Close to CNxx pin 14 & pin23
4.7u CAP close to pin23

5/10 change Card Redaer conn
footpirnt sdcard-sdsn09-08-xa-11p-smt



CTRL0, CTRL1 trace length shorter,
and surround with GND.



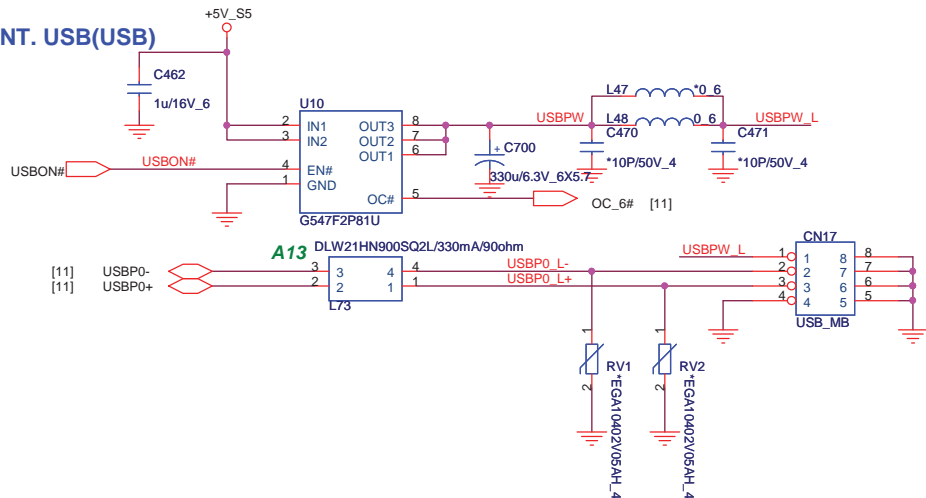
<http://hobi-elektronika.net>



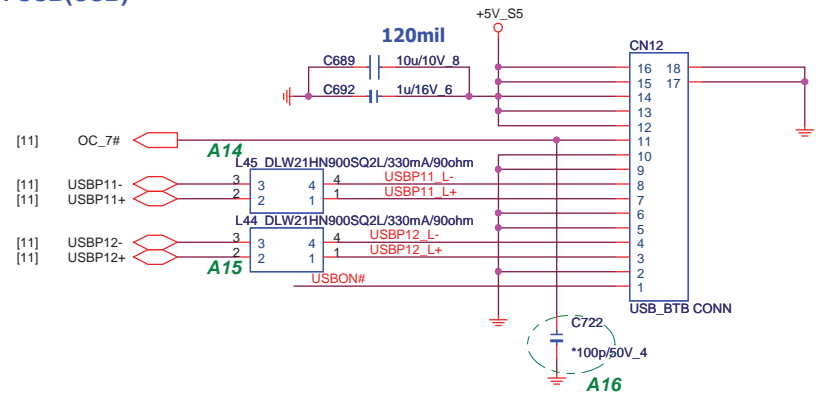
PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	AU6433 CardReader	1A
Date:	Monday, May 31, 2010	Sheet 30 of 48

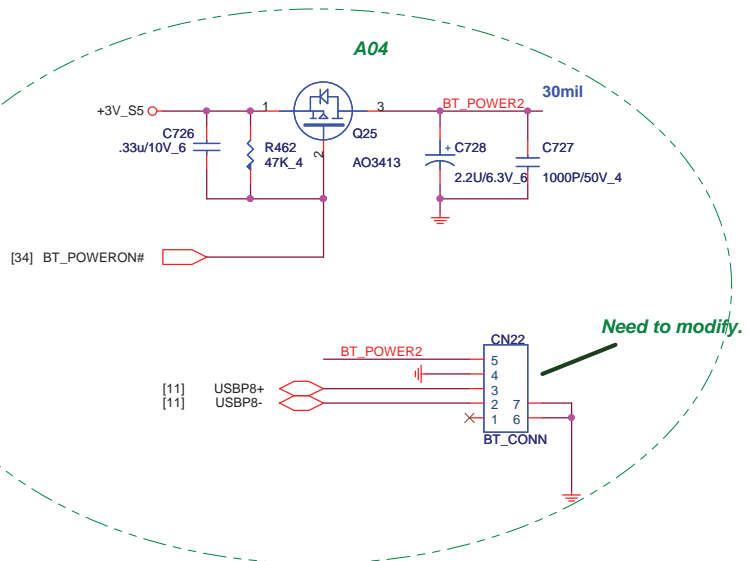
INT. USB(USB)



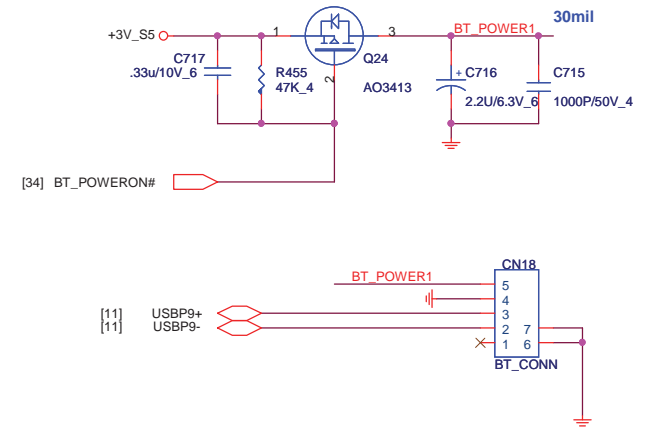
EXT. USB(USB)



BLUETOOTH V2.1 CONN(BTM)



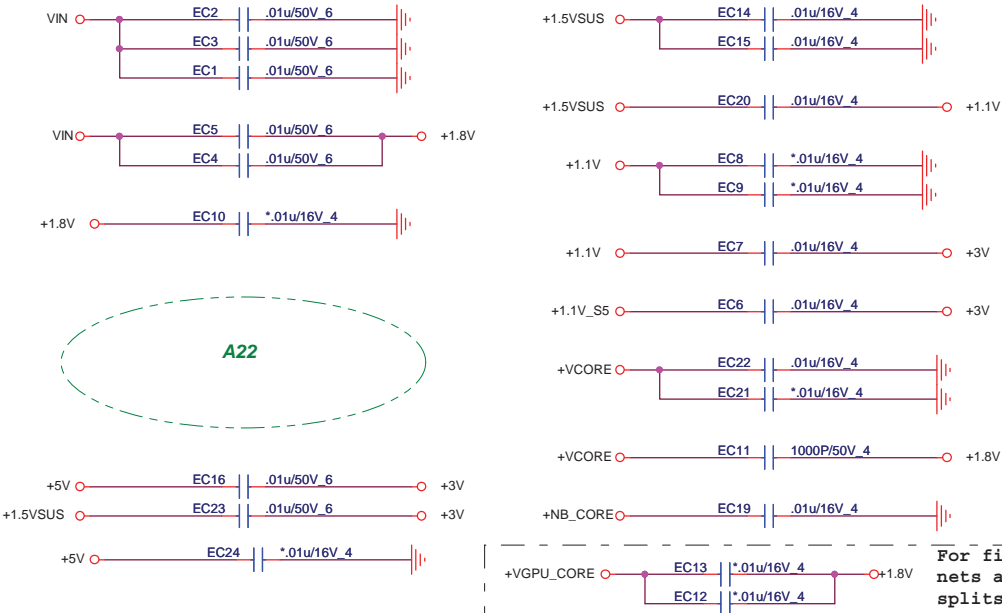
BLUETOOTH V3.0 CONN(BTM)



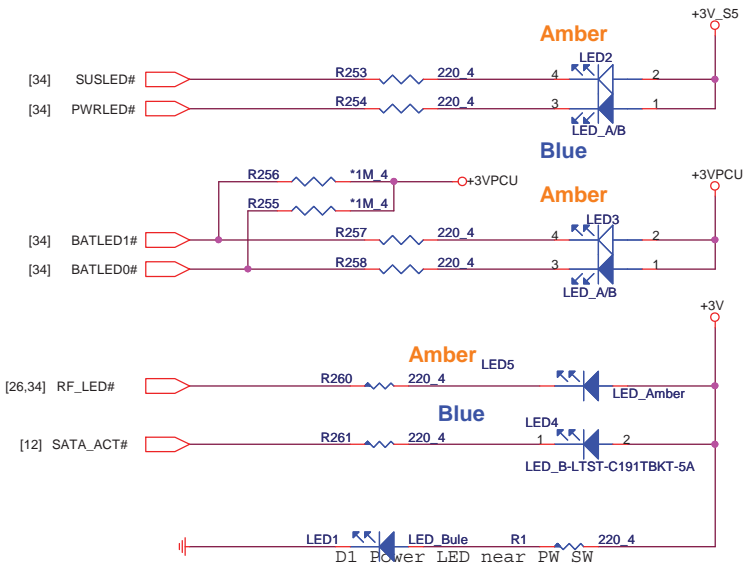
PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number USB/BT/TP	Rev 1A
Date:	Monday, May 31, 2010	Sheet 31 of 48

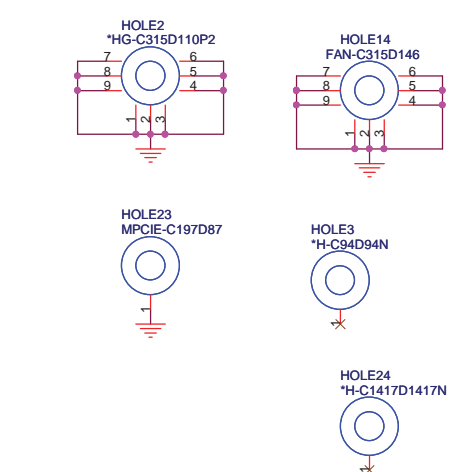
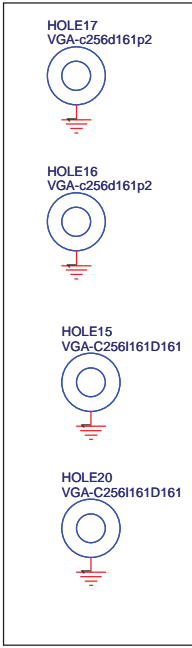
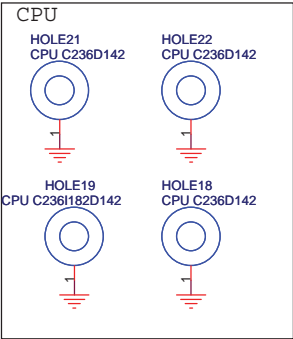
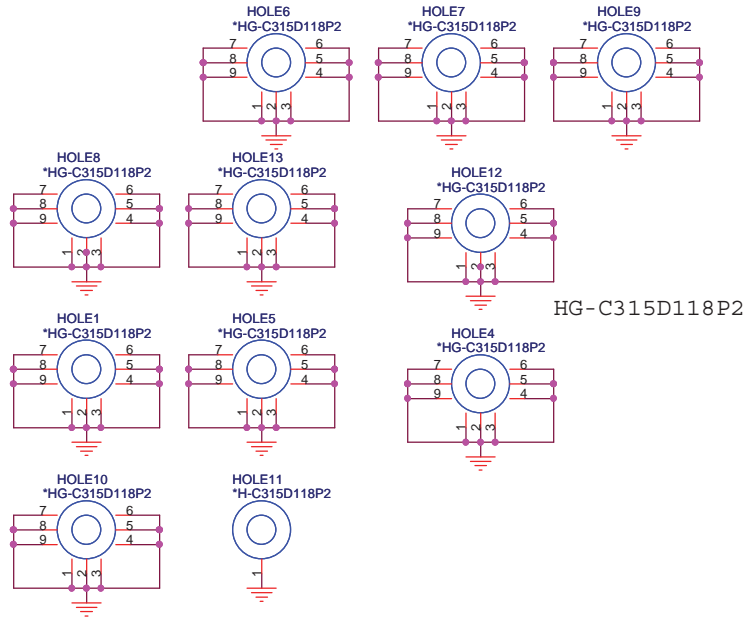
EE RETURN-PATH CAPACITORS(EMC)



LED(UIF)



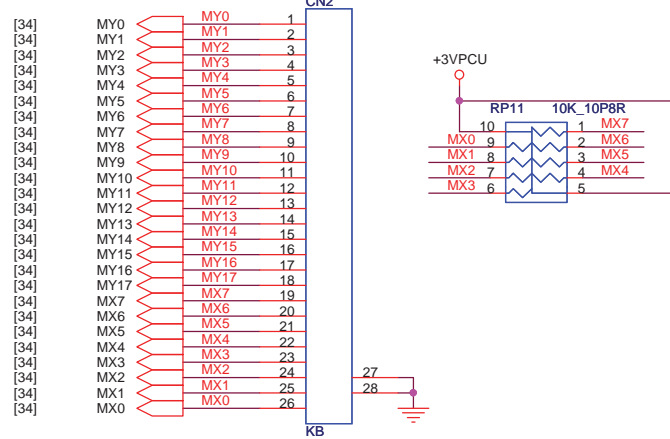
HOLE(OTH)



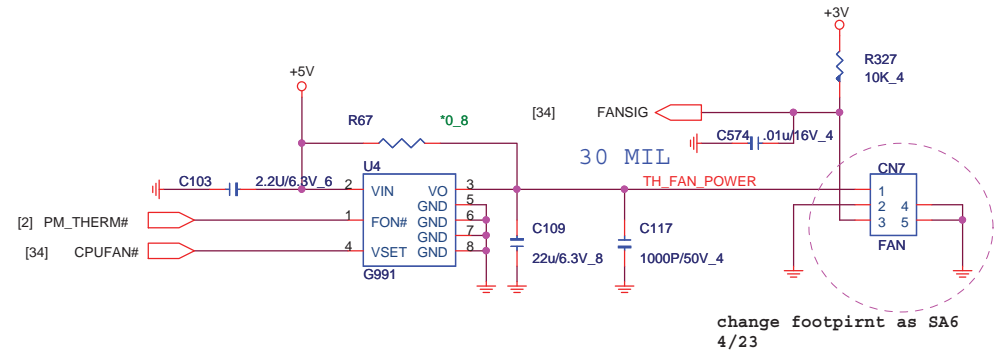
PROJECT : ZQA
Quanta Computer Inc.

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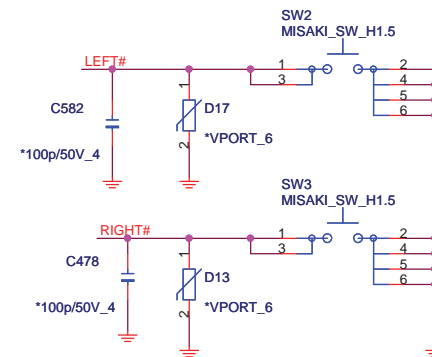
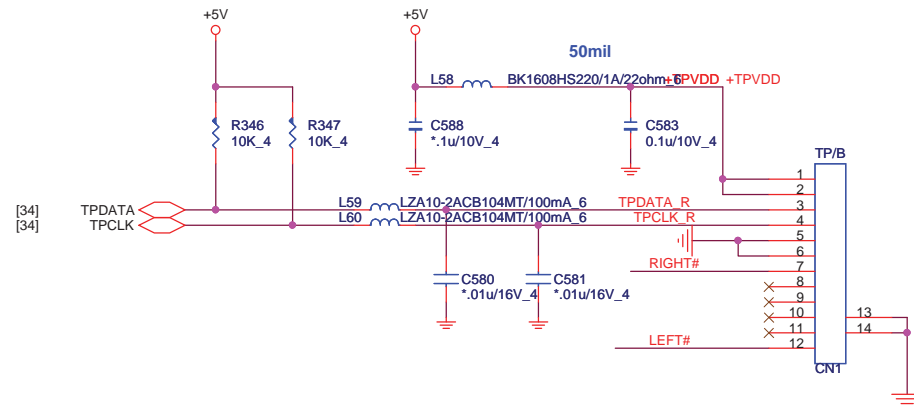
K/B(KBC)



CPU FAN(THM)



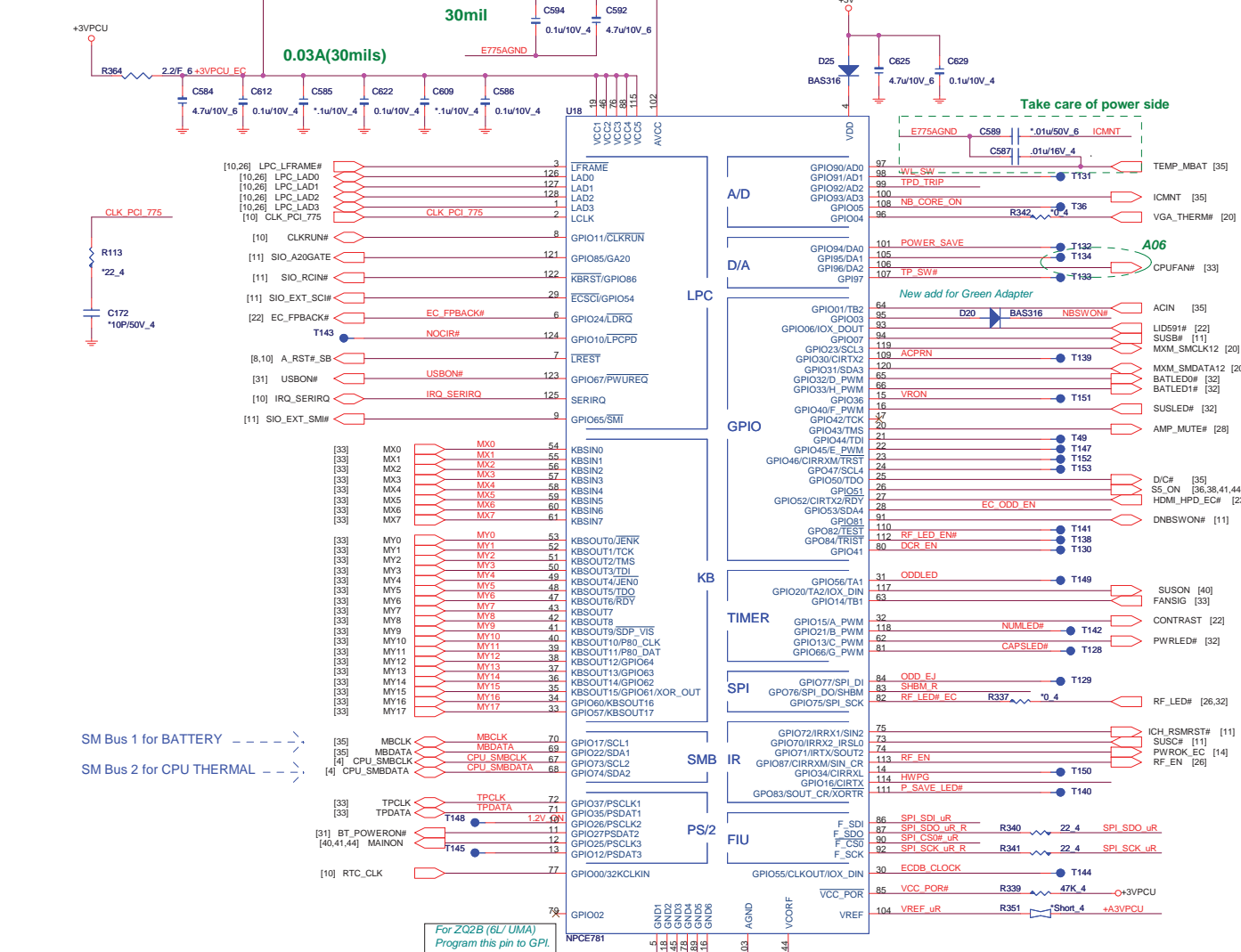
TOUCHPAD BOARD CONN(TPD)



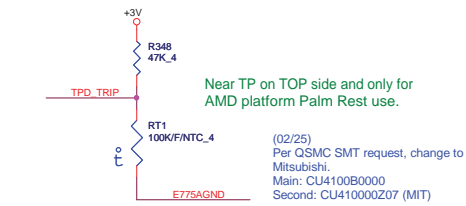
PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number KB/FAN/EE RETURN CAP	Rev 1A
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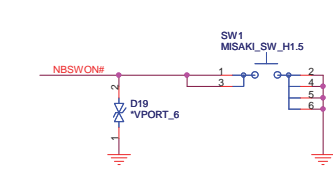
EC(KBC)



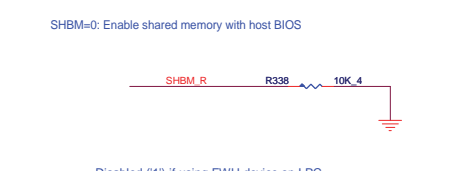
PALM REST THERMAL SENSOR (THM)



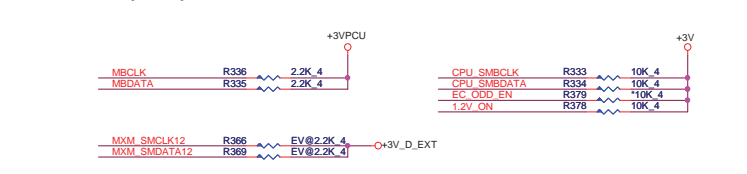
POWER-ON SWITCH (KBC)



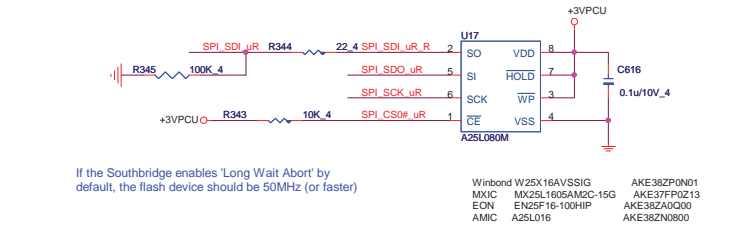
POWER-ON SWITCH (KBC)



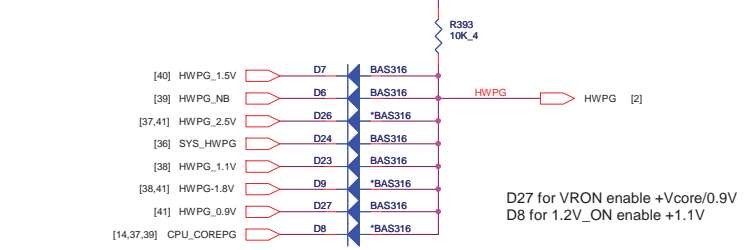
SM BUS PU(KBC)



SPI FLASH(KBC)



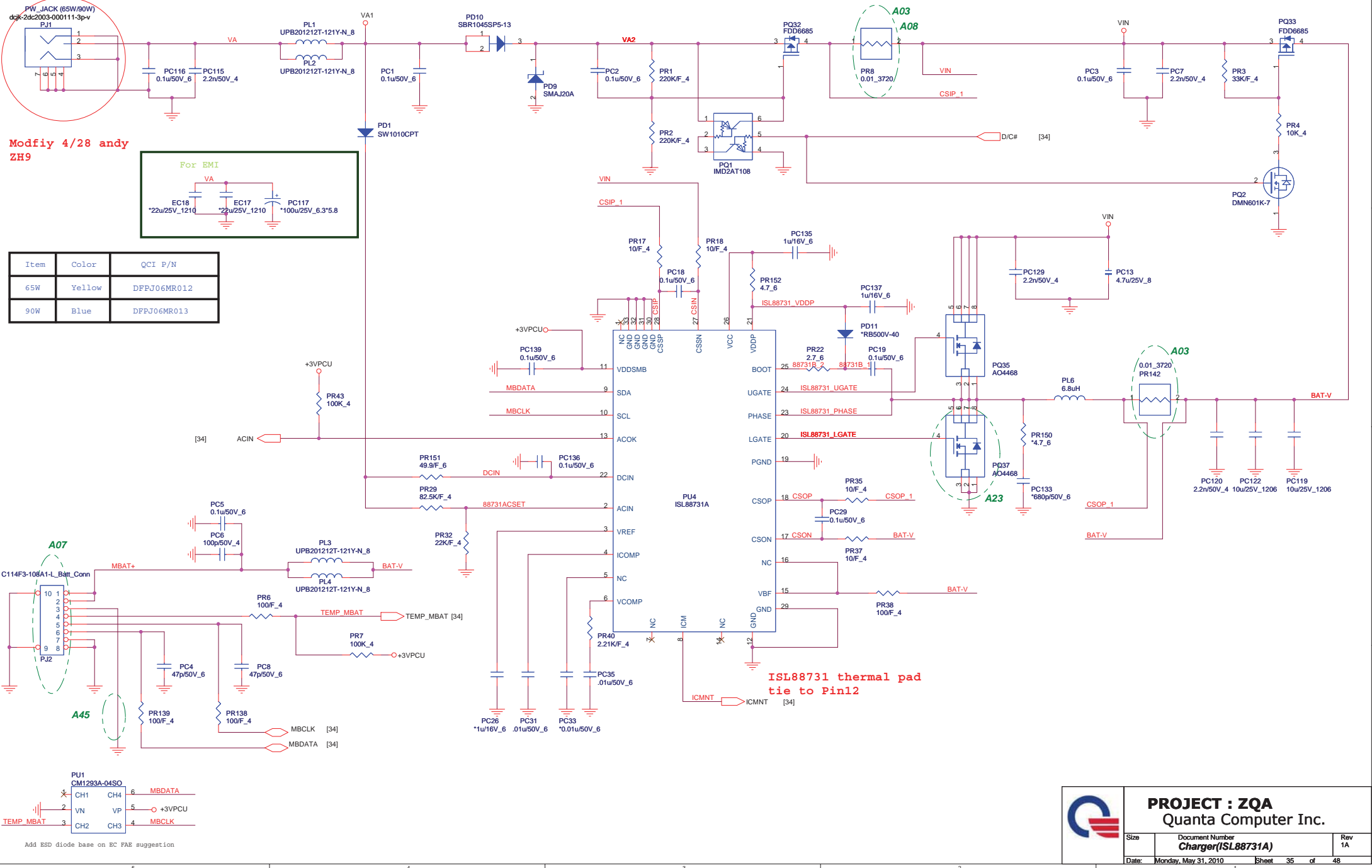
HWPG(KBC)



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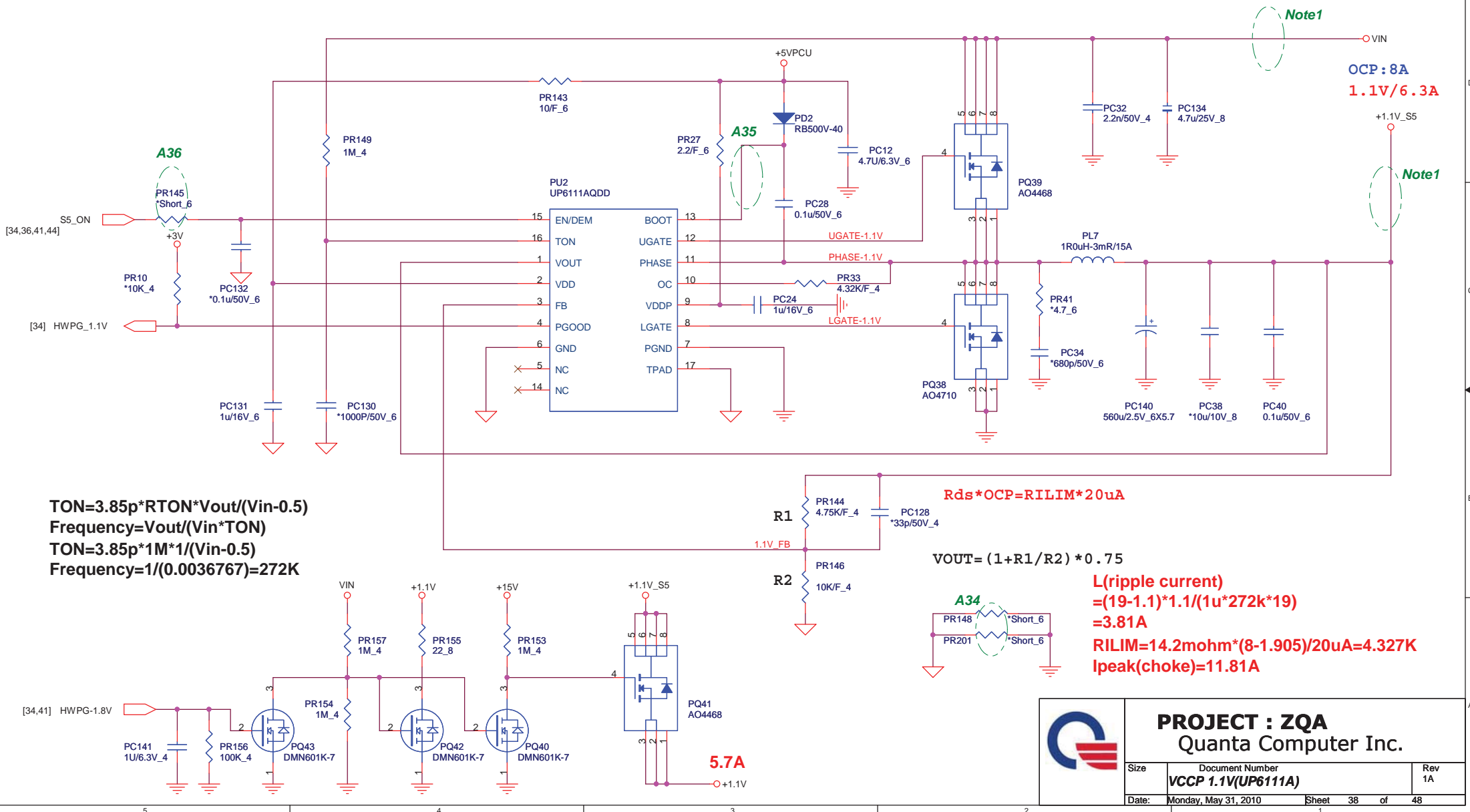
PROJECT : ZQA
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SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8






$TON = 3.85p \cdot R_{TON} \cdot V_{out} / (V_{in} - 0.5)$
 $Frequency = V_{out} / (V_{in} \cdot TON)$
 $TON = 3.85p \cdot 1M \cdot 1 / (V_{in} - 0.5)$
 $Frequency = 1 / (0.0036767) = 272K$

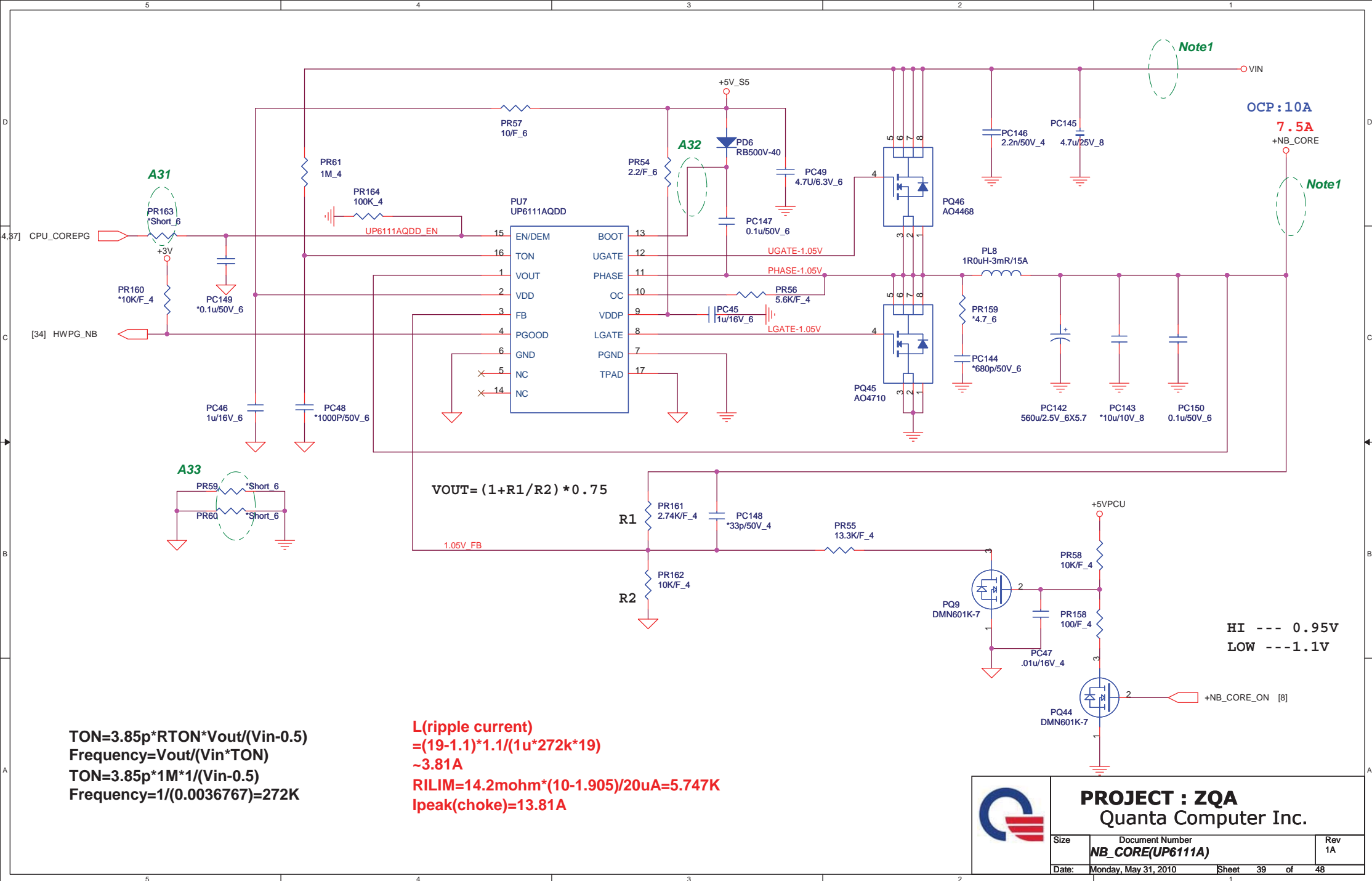
$R_{ds} \cdot OCP = R_{ILIM} \cdot 20\mu A$
 $V_{OUT} = (1 + R1/R2) \cdot 0.75$

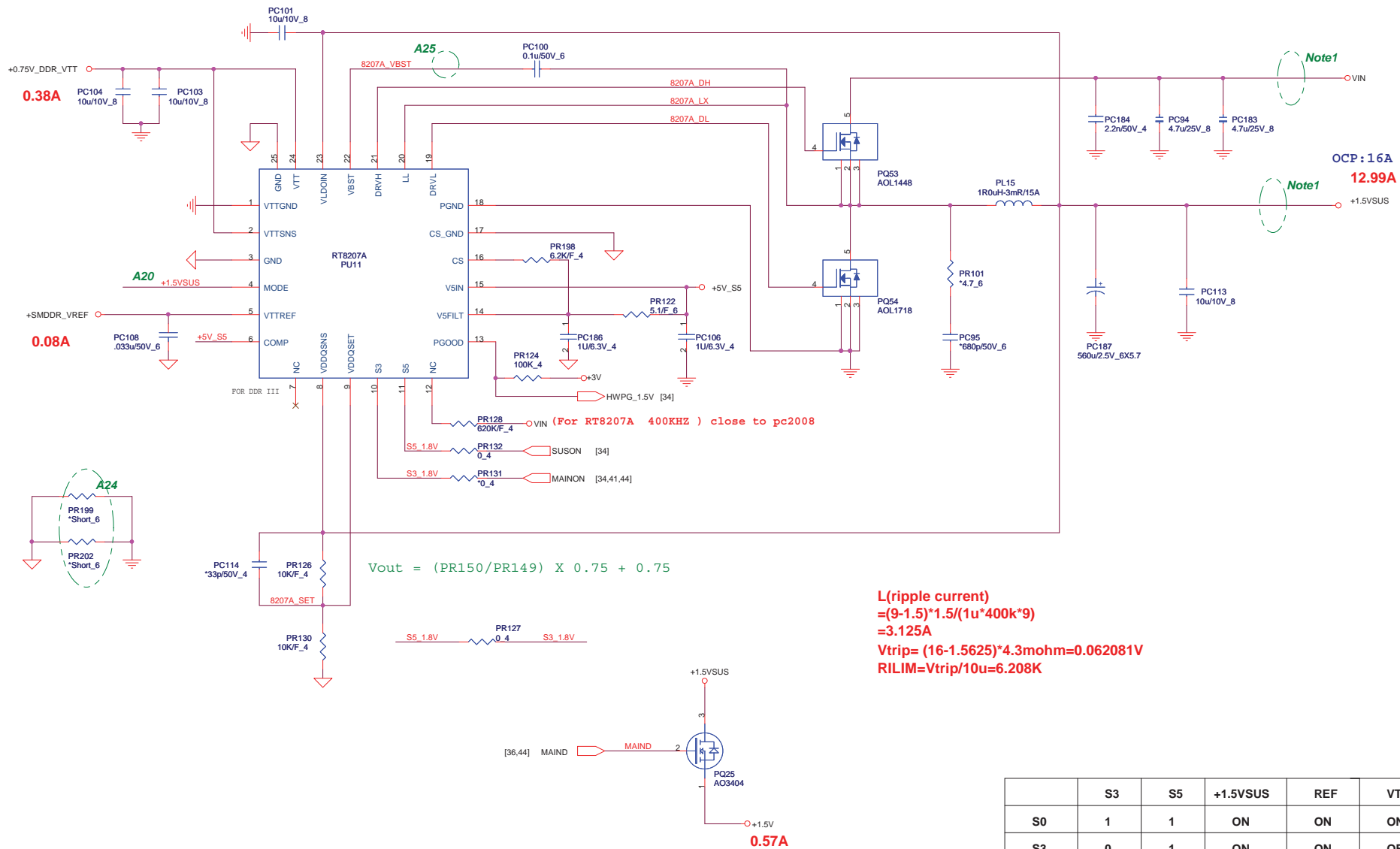
$L(\text{ripple current}) = (19 - 1.1) \cdot 1.1 / (1\mu \cdot 272k \cdot 19) = 3.81A$
 $R_{ILIM} = 14.2mohm \cdot (8 - 1.905) / 20\mu A = 4.327K$
 $I_{peak}(\text{choke}) = 11.81A$



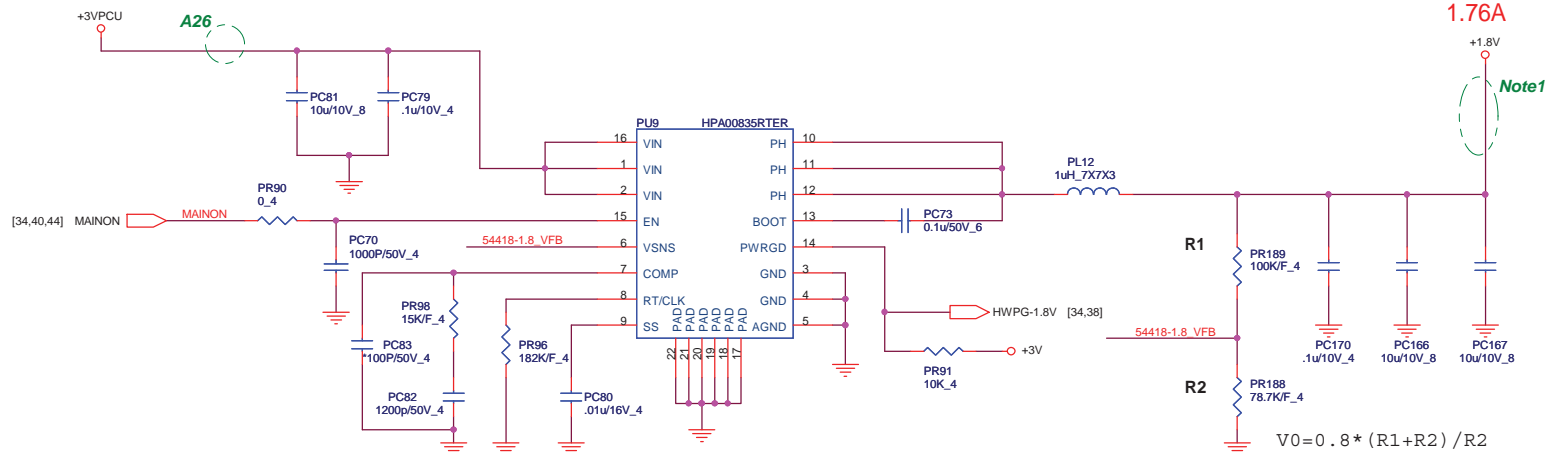
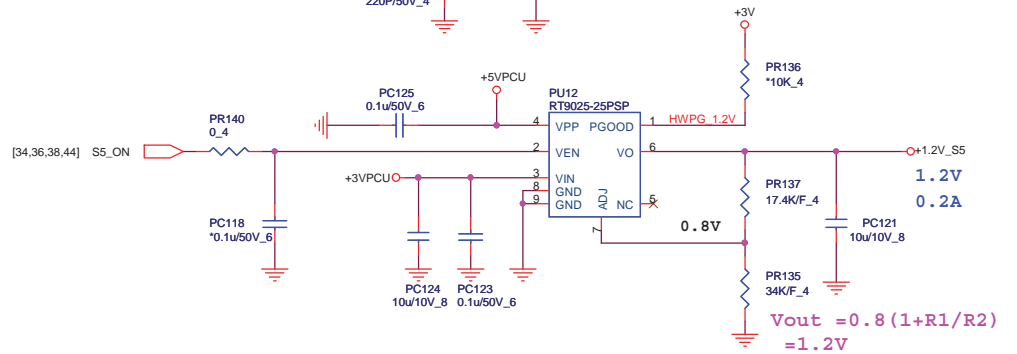
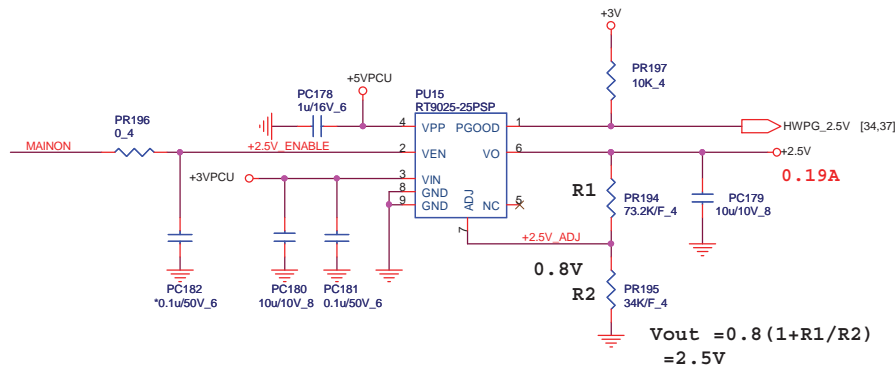
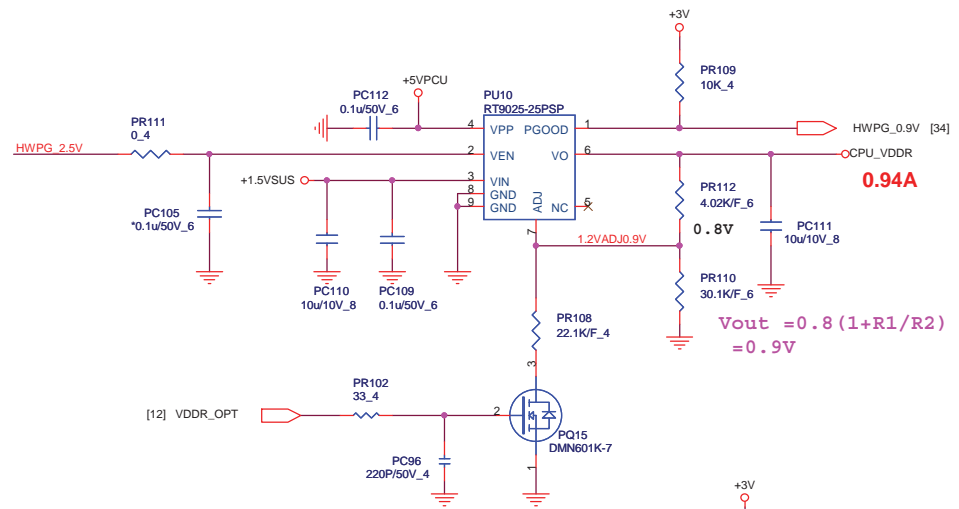
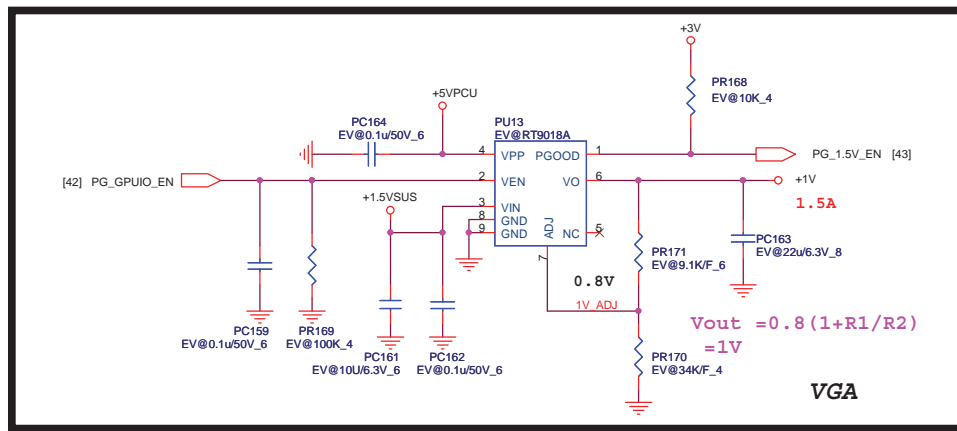
PROJECT : ZQA
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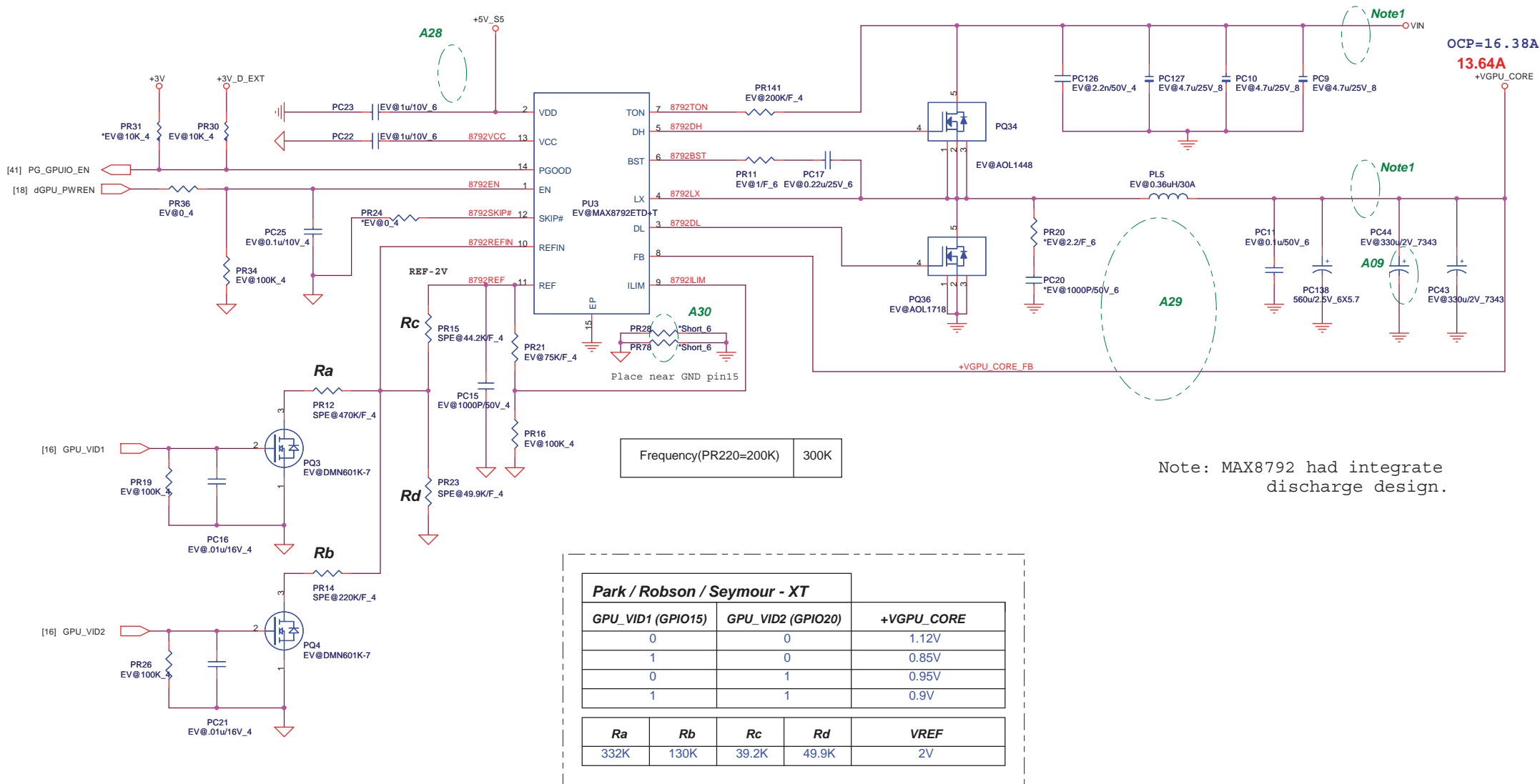




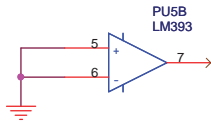
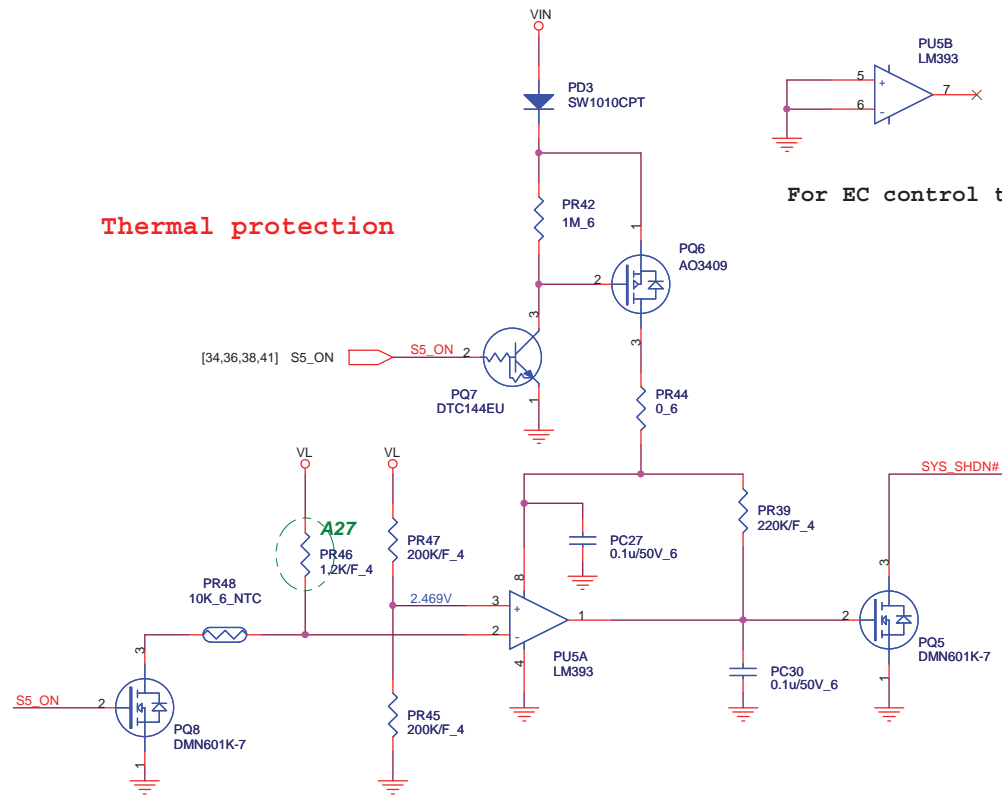
	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



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	LDO	1A
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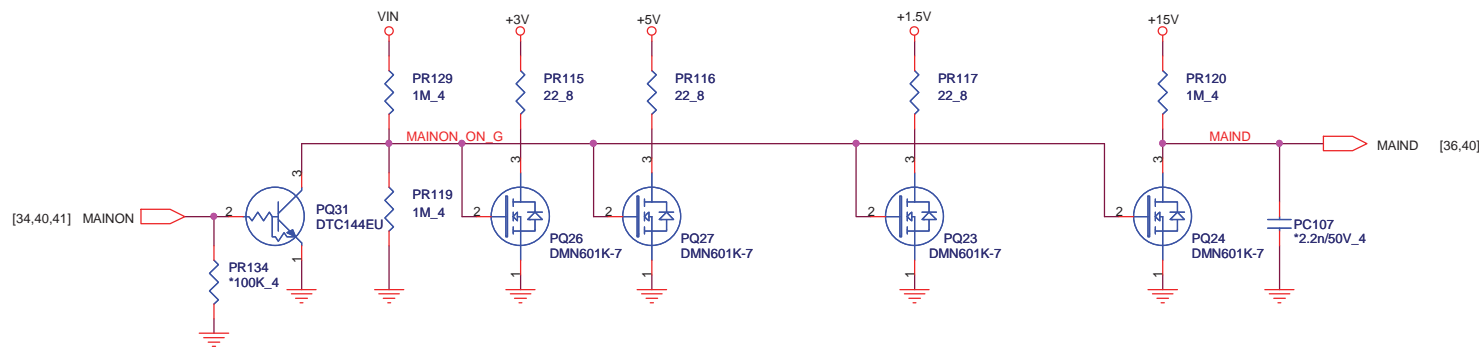
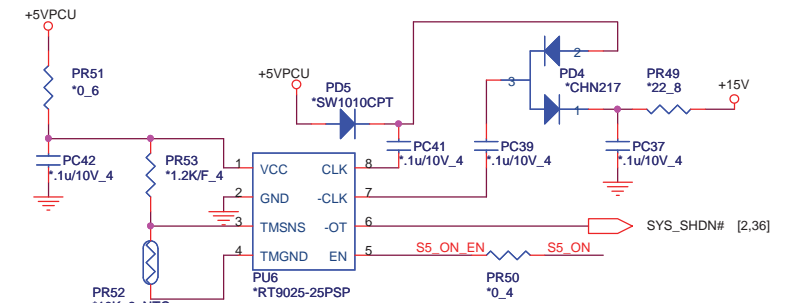


Thermal protection



For EC control thermal protection (output 3.3V)

POWER TEST : Thermal & Charge pump test circuit



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	Thermal protect	1A
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Power on Sequence required:

SB800:
1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS890:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3, +1.1V ramp before VCC_NB

SB OUTPUT - -NB_PWRGD
SB INPUT - -SB_PWRGD_IN

GROUP B
HWPG_0.95V
NB_CORE
+1.1V
CPU_COREPG
CPU_VDDR
+VCC_CORE
CPU_VDDNB_CORE

GROUP A
HWPG_2.5V
+2.5V (CPU_VDDA_2.5_RUN)
+1.5V
HWPG_1.8V
+1.8V
+5V/+3.3V
MAIN_ON
SUSB#
VDRAM_PWRGD
+0.75V_DDR_VTT
+SMDDR_VREF
+1.5V_SUS

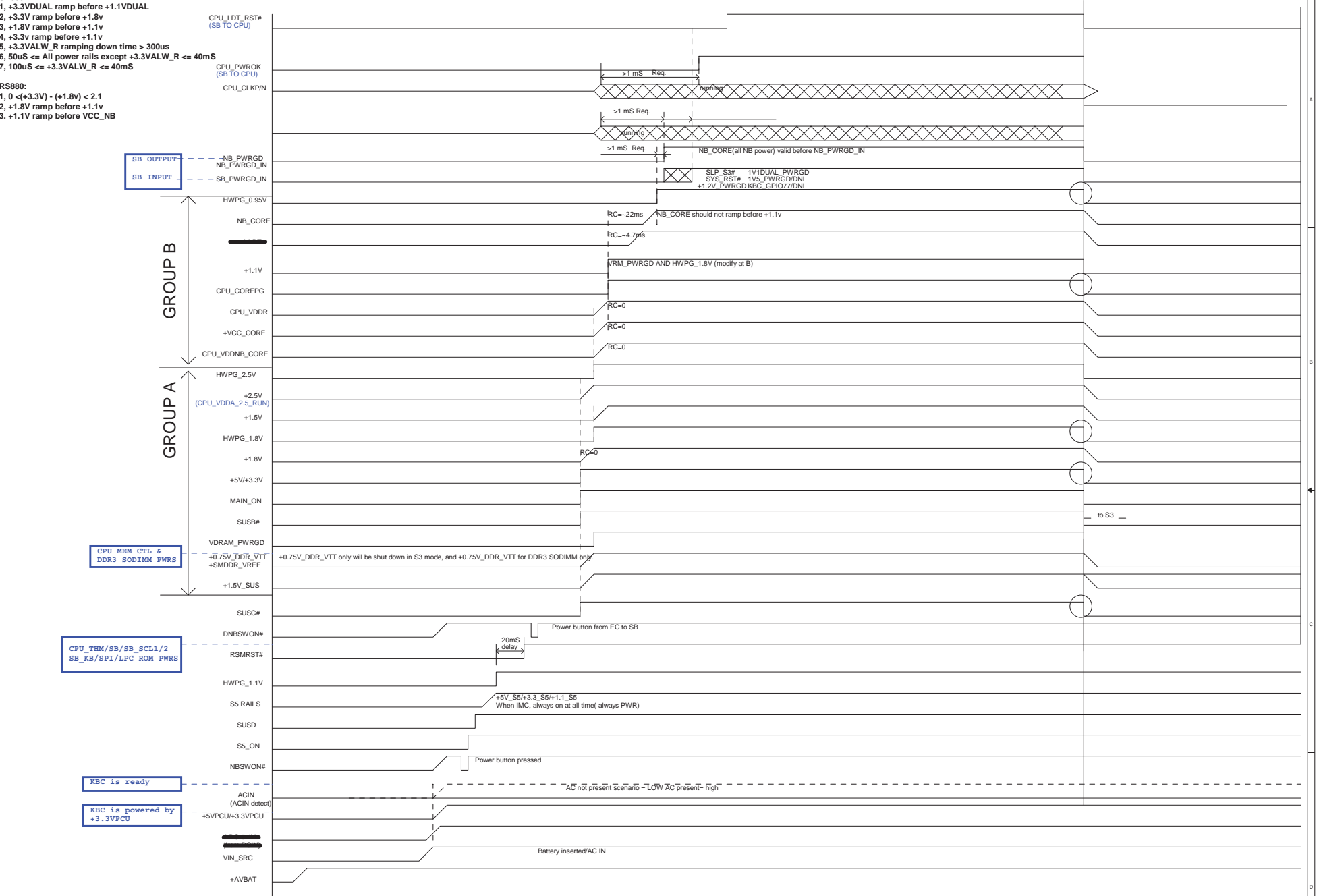
CPU THM/SB/SCL1/2
SB_KB/SPI/LPC ROM PWRS

KBC is ready

KBC is powered by +3.3VPCU

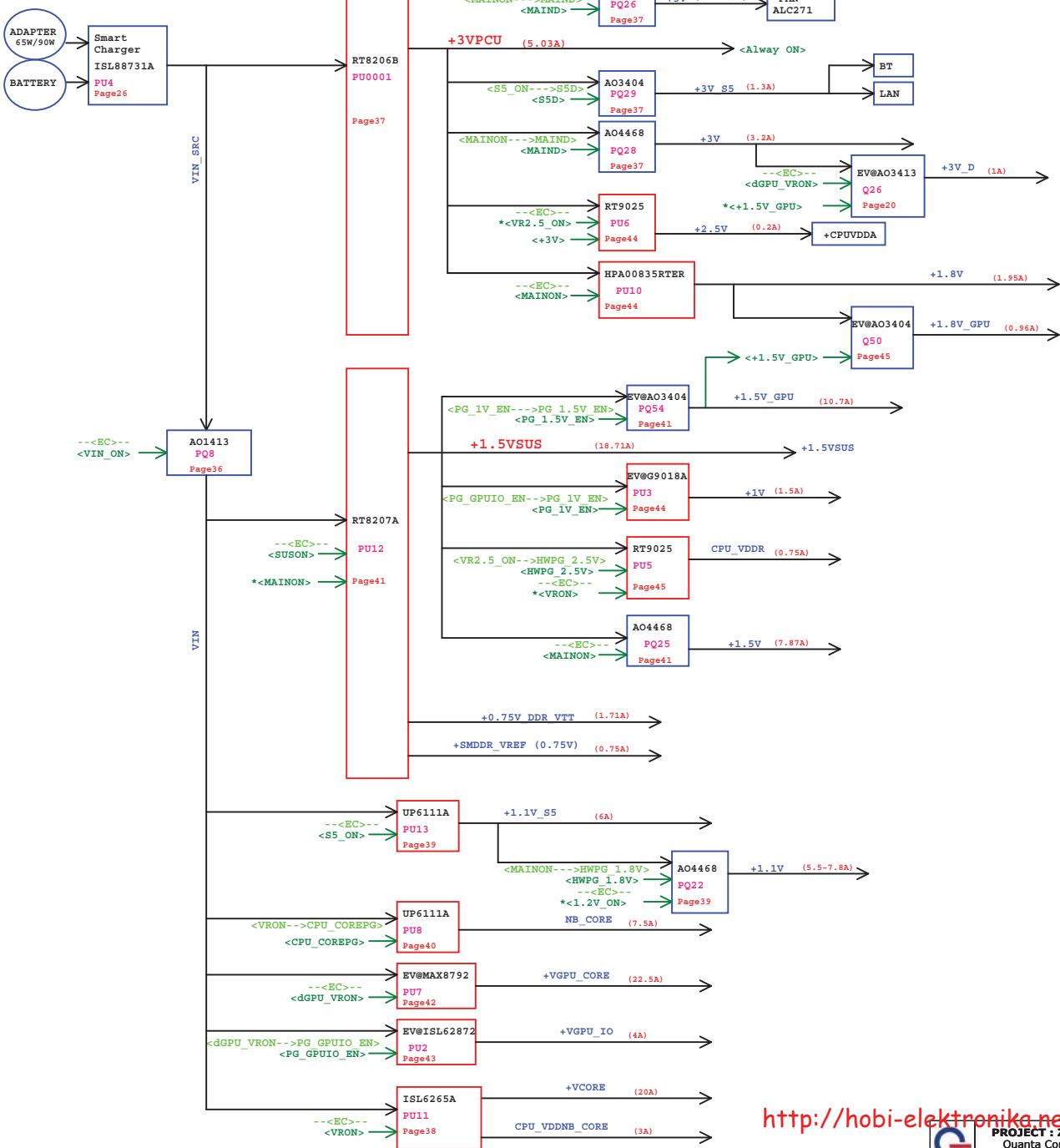
VIN_SRC

+AVBAT

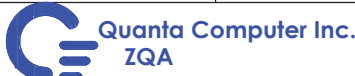




ZQ2B Power tree



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MODEL	REV	CHANGE LIST	Model	KN1A M/B BOARD	
			Page	From	To
ZQA M/B	3A	<p>A01 PAGE28 : Add pull high resistor 4.7kohm on PD# pin, the reason is prevent speaker no sound.</p> <p>A02 PAGE28 : Change R229,R223 to 33K for speaker 1W.</p> <p>A03 PAGE35 : Change PR8,PR142 from 1m ohm to 10m ohm.</p> <p>A04 PAGE31 : Add BT2.1 design for Customer request.</p> <p>A05 PAGE22 : Delete R8 bead.</p> <p>A06 PAGE34 : The connection of CPUFAN# is changed from 105pin to 106pin.</p> <p>A07 PAGE35 : Change P/N</p> <p>A08 PAGE35 : Change PR8 Package to 3720</p> <p>A09 PAGE42 : Stuff PC44</p> <p>A10 PAGE37 : Stuff PC165</p> <p>A11 PAGE37 : Stuff PC153</p> <p>A12 PAGE36 : Change P/N</p> <p>A13 PAGE31 : Stuff L73</p> <p>A14 PAGE31 : Stuff L45</p> <p>A15 PAGE31 : Stuff L44</p> <p>A16 PAGE31 : Add 100p for EMI</p> <p>A17 PAGE23 : Add 1000p for EMI</p> <p>A18 PAGE23 : Add 1000p for EMI</p> <p>A19 PAGE02 : Delete R356</p> <p>A20</p> <p>A21</p> <p>A22 PAGE32 : Delete EC25,EC26,EC27,EC28</p> <p>A23</p> <p>A24</p> <p>A25</p> <p>A26</p> <p>A27 PAGE44 : Change PR46 from 1.7K ohm to 1.2K ohm.</p> <p>A28</p> <p>A29</p> <p>A30</p> <p>Note :</p> <p>1. Remove Jumper : JP5,JP16,JP6,JP14,JP3,JP13,JP11,JP2,JP8,JP9,JP10,JP15,JP17,JP12,JP1,JP7</p> <p>2. Remove 0 ohm :</p> <p>R355,R356,R370,183,R207,R73,R331,L61,R76,R65,R83,R42,R50,L9,R35,R24,R27,R448,R228,R204,R202,R199,R197,R195,R223,R424,R414,R400,R442,R459,R458,R446,R62,R70,R351.</p> <p>3. Change footprint :</p> <p>C119,C139,C149,C153,C154,C181,C182,C185,C191,C192,C195,C198,C199,C201,C202,C204,C205,C209,C217,C218,C222,C224,C225,C233,C234,C235,C236,C242,C248,C249,C252,C255,C260,C261,C262,C263,C266,C268,C270,C273,C275,C277,C280,C285,C304,C307,C313,C314,C316,C318,C328,C329,C330,C332,C335,C336,C337,C338,C340,C361,C362,C363,C364,L30,L39,R9,R84,R89,R95,R96,R98,R123,R126,R134,R158,R363,C296,C308,C213</p>	1	1A	3A
			2	1A	3A
			3	1A	3A
			4	1A	3A
			5	1A	3A
			6	1A	3A
			7	1A	3A
			8	1A	3A
			9	1A	3A
			10	1A	3A
			11	1A	3A
			12	1A	3A
			13	1A	3A
			14	1A	3A
			15	1A	3A
			16	1A	3A
			17	1A	3A
			18	1A	3A
			19	1A	3A
			20	1A	3A
			21	1A	3A
			22	1A	3A
			23	1A	3A
			24	1A	3A
			25	1A	3A
			26	1A	3A
			27	1A	3A
			28	1A	3A
			29	1A	3A
			30	1A	3A
			31	1A	3A
			32	1A	3A
			33	1A	3A
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			39	1A	3A
			40	1A	3A
			41	1A	3A
			42	1A	3A
			43	1A	3A
			44	1A	3A
			45	1A	3A
			46	1A	3A
			47	1A	3A
			48	1A	3A
		PROJECT: ZQA	PCBA NO. http://hobi-elektronika.net	DOC. NO :	
APPROVED BY : Johnny O		CHECK BY : Darren Liao	DRAWING BY : Bowen Chuang	DATE :06/11/2010	SHEET 1